Mauna Kea Infrared
FCRYO2 Fiber Interface Subassembly

MKIR# 700-200-01
Rev 0.71 (PRELIMINARY)
Last Modified 10/19/04

WARNING: **The FCRYO2 board is not compatible with the VME standard**, though it may appear to be. Inserting the FCRYO2 in a standard VME chassis will likely cause a **catastrophic failure**. Likewise inserting standard VME cards into the chassis is prohibited and extremely risky.

Revision History

Revision	Author	Summary of revisions	Date
0.71 PRELIM	Mike Thompson	Initial release to customer.	10/19/04
0.3	Peter Onaka	Source revision.	2/14/02

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1 FCRYO2 Overview

This document specifies the functionality and use of the Fiber Interface Subassembly, FCRYO2. The FCRYO2 board is a component of the Redstar3 Array Controller. Redstar3 boards are housed in a 63HP Eurocard chassis called an Array Control Chassis. The FCRYO2 contains three modules, the Clocker, the Catcher, and an SL240 CMC fiber interface (for Frame Data). The Catcher and Clocker are implemented in Brightstar IPEngines.

The FCRYO2 provides several functions. It is the interface to the control and processing computers of the Redstar3 for the array control electronics. Three fiber interfaces are provided for communicating with the Redstar3's Instrument Controller and Pixel Server. The link to the Pixel Server is a high-speed 2.5Gbps FPDP fiber link. The links to the Instrument Controller are 10 Mbps Ethernet links converted to fiber. Fiber links to the Pixel Server and Instrument Controller provide optical isolation which allows for complete ground separation between the Instrument Controller, Pixel Server, and the Array Control electronics. This helps minimize any noise the Array Controller could introduce into the data streams.

The FCRYO2 generates digital clocks for clocking an imaging array. The FCRYO2's Clocker generates digital clocks that are driven over the Array Control Chassis backplane to the Redstar3's CLKBIAS boards. The FCRYO2 also provides a TTL trigger for synchronizing array readouts with signals from the facility's system.

The FCRYO2 board's Catcher takes digital pixel data from the Array Control Chassis' backplane, buffers it, and sends the data on to the SL240 CMC fiber interface modules for transmission to the Pixel Server.

A photo of the FCRYO2 board is provided in Figure 3.

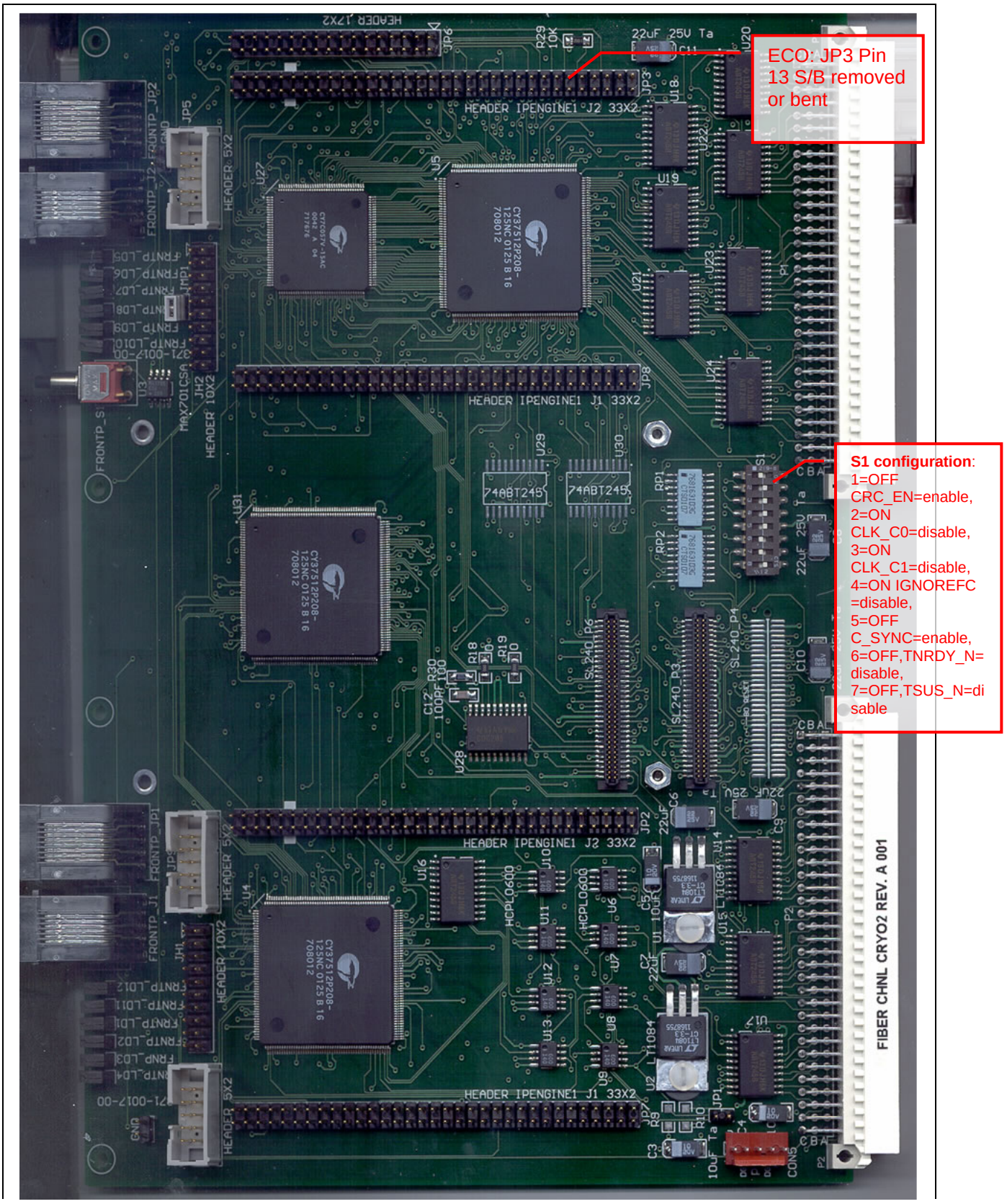

Figure 1 Photo: FCRYO2 board without IPEngine and SL240 Daughter Cards

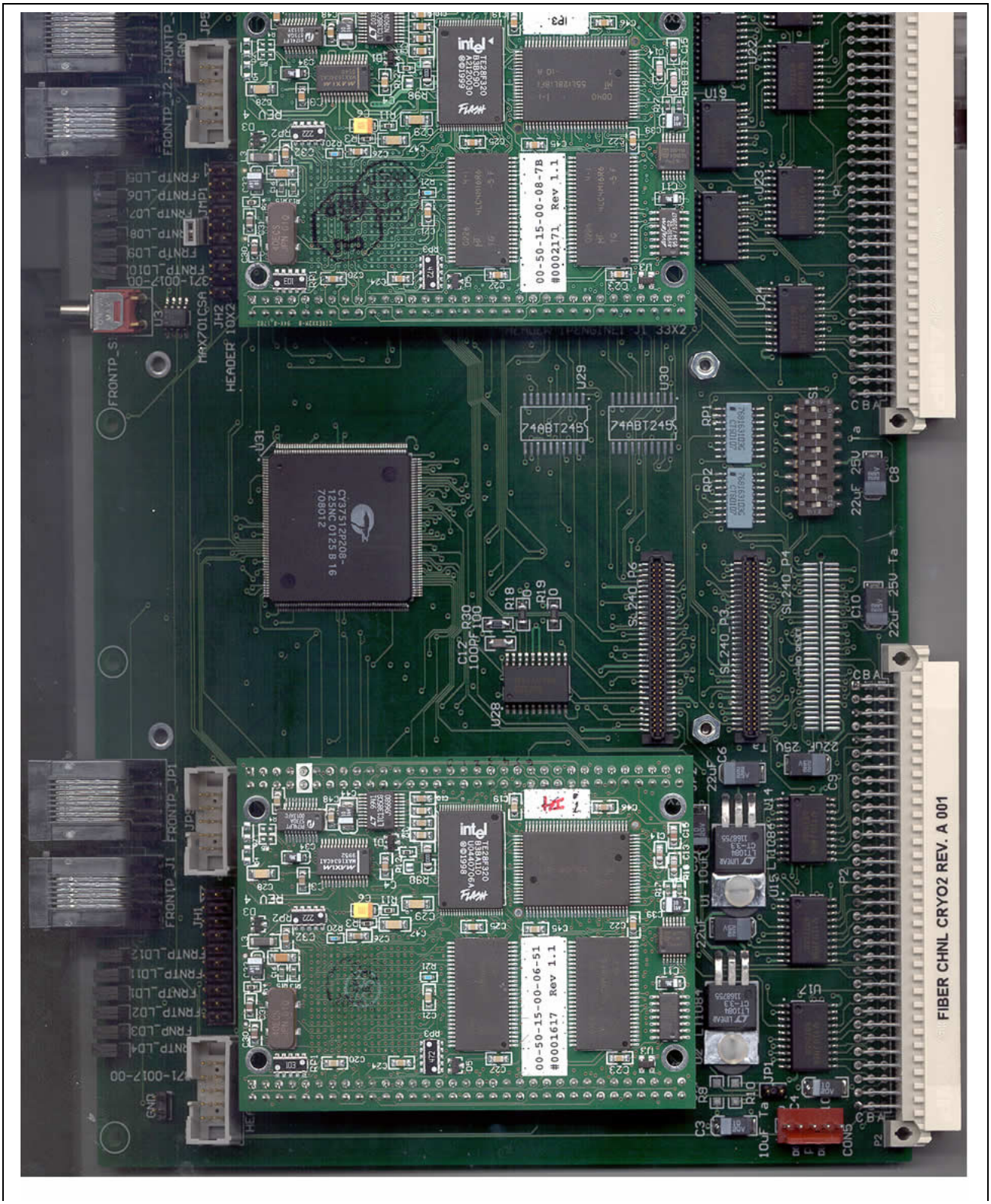

Figure 2 Photo: FCRYO2 Board without SL240 Daughter Card

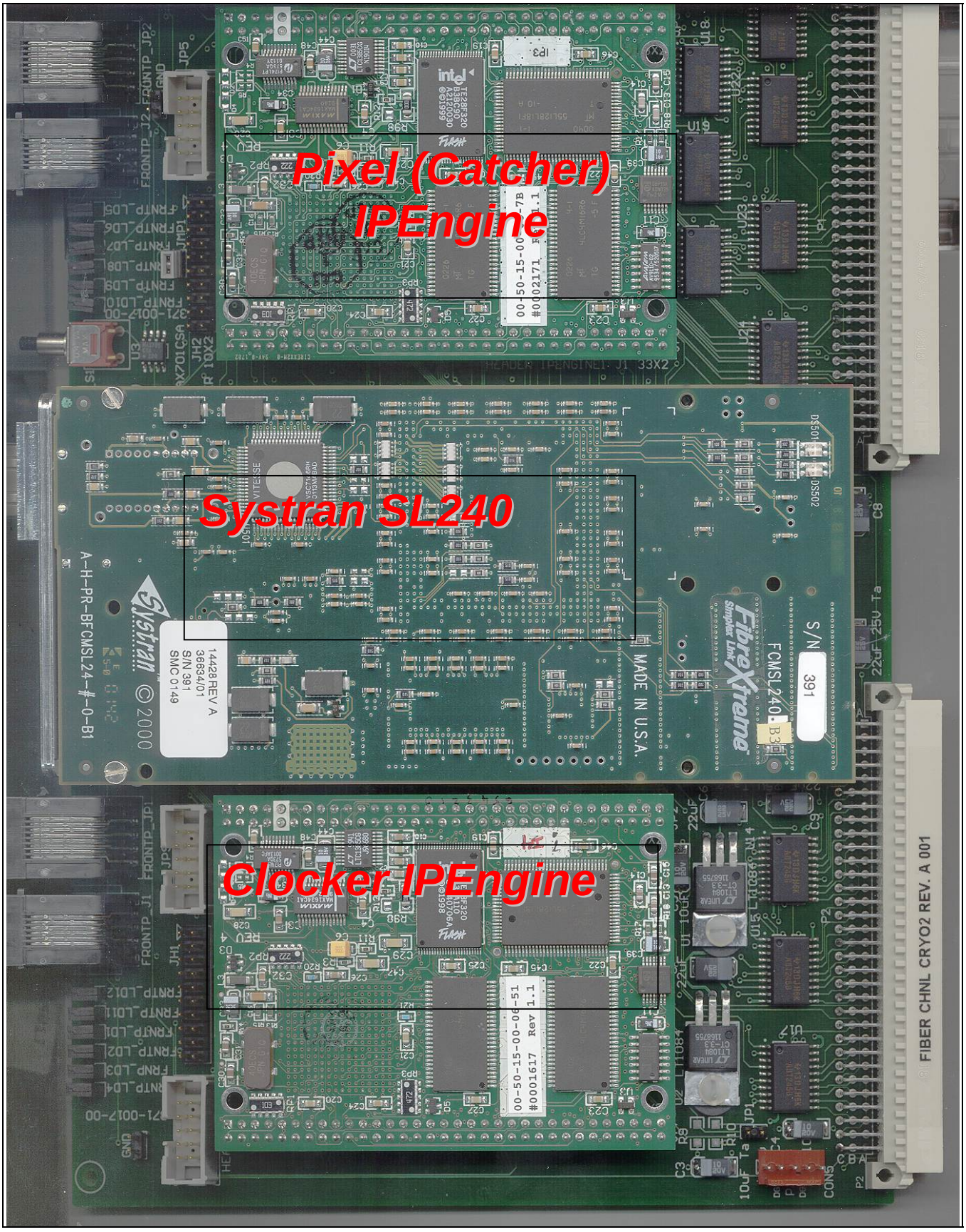

Figure 3 Photo: Component Side of FCRYO2 Board with Daughter Cards

2 Technical Specifications

This section provides a quick overview of the technical features of the FCRYO2.

2.1 General Technical Specifications

FCRYO2

- Front panel LEDs for status
- 8 layer PCB

High Speed Fiber Link

- Full 2.5Gbps Systran FibreXtreme SL240 CMC, PCI to FPDP transmit/receive channels
- 300m fiber range
- LC fiber connector interface
- Uses FPDP (VITA 17.1) 32 bit data interface to Fiber Channel based link
- 8b/10b encoding
- 247Mbytes/sec max throughput with or without checksum
- 1 MB receive FIFO
- 4 kB transmit FIFO
- Status LED
- 850nm wavelength laser Class 1, eye safe
- CMC physical format
- 50um or 62.5 core fiber
- Weight ~ 0.25lbs
- Dimensions: 2.91x 5.87 inches (74 x 149 mm)
- Power dissipation 8.2W average
    - +5VDC, 0.9 Amps av., 1.3 Amps peak
    - +3.3VDC, 1.1 Amps av. and peak

Embedded Ethernet Connected LINUX Control

- 2 embedded Brightstar IPEngine1 PowerPC+FPGA boards for Clocking and fiber communication
- Each IPEngine1
    - 10BT Ethernet interface
    - LINUX OS running on a 48MHz PowerPC
    - 1Mx16 FLASH RAM
    - 16,000 gate Altera FPGA EP6016
    - 128kx16 Sync SRAM
- Clocking FPGA
    - Patterns
        - 7 x 1/48Mhz = 145.83nsec min pattern time
        - 1/48Mhz = 20.8333nsec pattern time extension
        - 10 bit pattern run length extension = 21.313usec
    - Rows and frames
        - 10 bit rep count = 1024 times
    - integration timer
        - 25usec time increments
        - 28 bit timer = 3.728 hrs max ITIME
- Power dissipation 25mW to 2W app dependent
    - +5V DC ± 5% 800mA Typical

2.2 Power Requirements

- +5V 2.2A Typ.

2.3 Mechanical Specifications

- Eurocard 6U (160mm x 233.35mm) Form Factor
- P1 96 pin DIN Connector,P2 DIN 41612, 96 Pin Connector
- 6 Layer PCB Construction with Internal Gnd & Power Layers

3 Functional Description

The FCRYO2 contains three modules, the Clocker, the Catcher, and an SL240 CMC fiber interface (for Frame Data). The Catcher and Clocker are implemented in Brightstar IPEngines. This section specifies the functionality and use of the FCRYO2 and its modules.

Both the Catcher and the Clocker have a 10 Mbps Ethernet link to the Redstar3's Instrument Controller. The SL240 provides a high speed FPDP fiber link (SL240 CMC), Frame Data, to the Pixel Server. Frame Data from images captured from the array are passed over this link to the Pixel Server for further processing.

The following is a qualitative description of the control and information flow through the FCRYO2. See Figure 5 for a block diagram of the FCRYO2.

Upon power up, FPGA images are written to the Clocker and Catcher IPEngines via the Clocker ENET and Catcher ENET fiber links. The Instrument Controller then writes array clocking patterns to the Clocker over the Clocker ENET fiber link. The Clocker, when armed and triggered, drives these digital clock patterns over the Array Control Chassis backplane's Clock Control Bus to the CLKBIAS boards. Two identical Clock Control Buses are driven out of the FCRYO2 board to the backplane. Subsequent digital array readout data is passed to the FCRYO2 via two 16 bit data streams from the Read Data Bus on the backplane. The Catcher buffers this data and passes it to the SL240 CMC for high speed transmission to the Pixel Server.

A system level view of the FCRYO2 board, indicating the peripheral devices with which it communicates, is provided in Figure 4. Note that this diagram is representational. Some system components and interconnects are not shown.

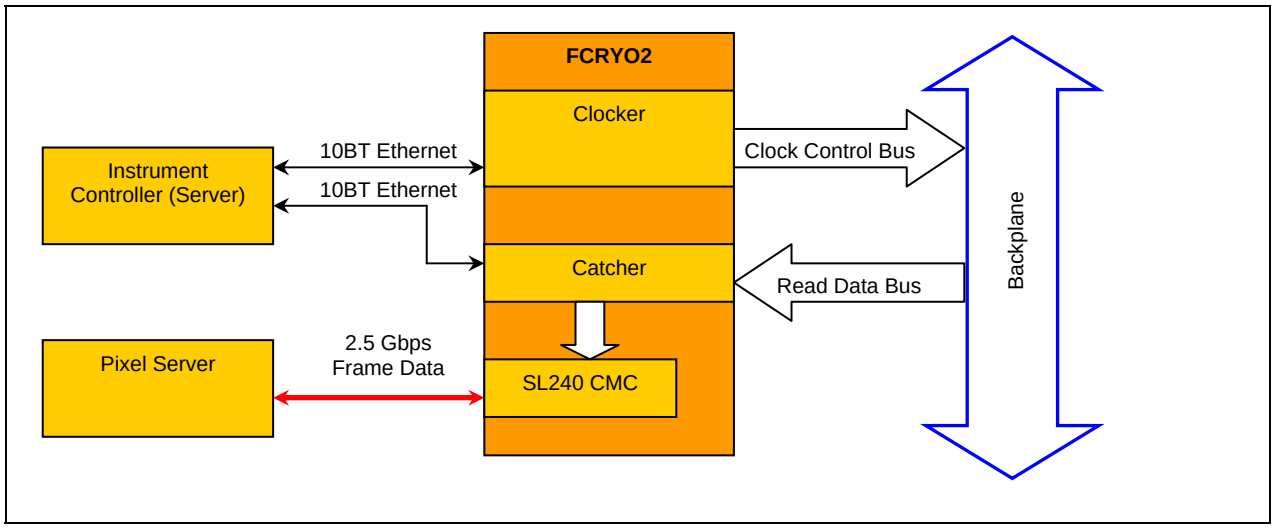

Figure 4 System Level View of the FCRYO2 Board

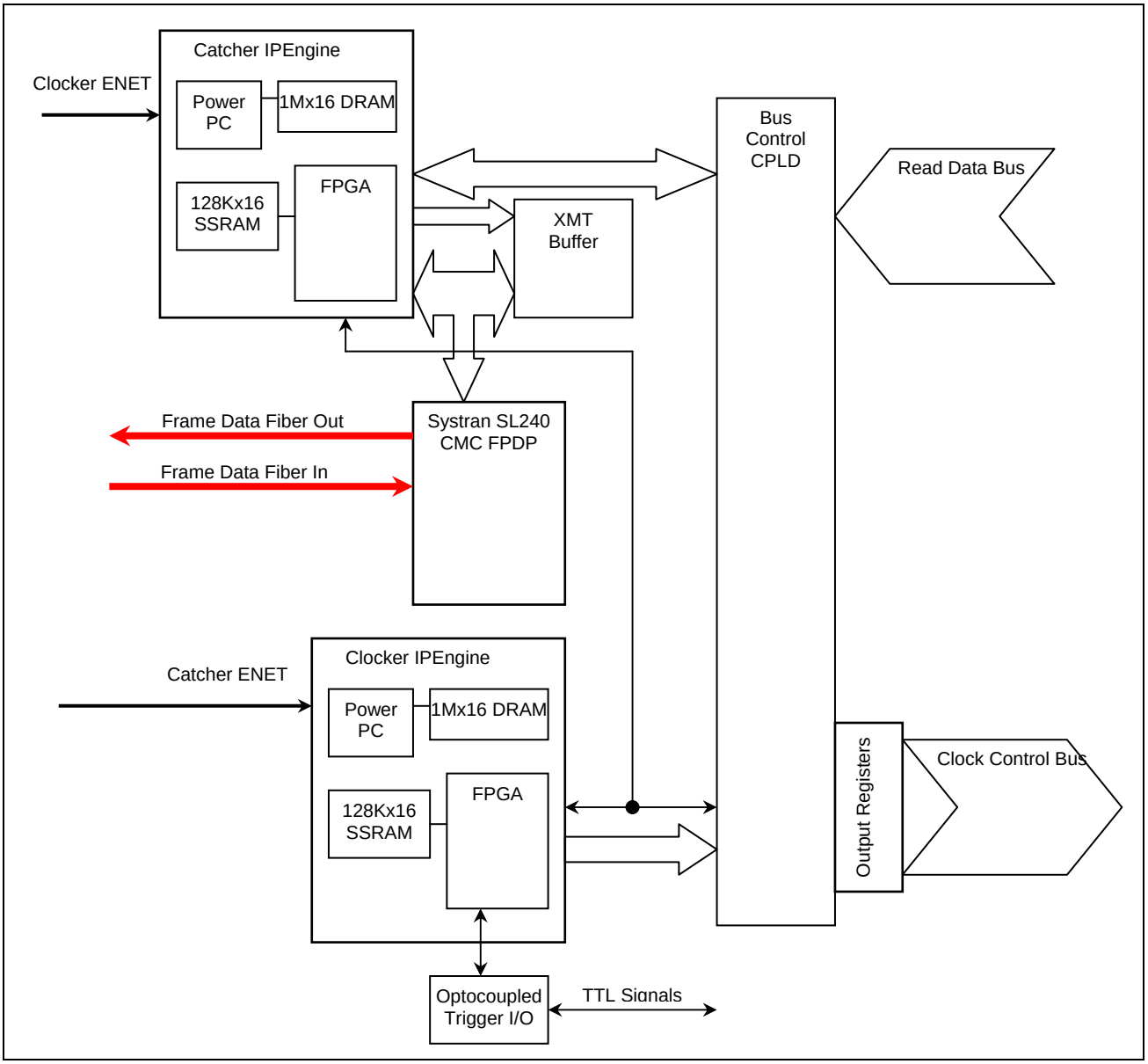

Figure 5 FCRYO2 Block Diagram

3.1 Frame Data-Fiber Optic Input/Output

The FCRYO2 has 2 LC fiber optic connectors from the Systran SL240 CMC fiber optic transceiver facing the front panel. The link provides a high-speed 2.5Gbps FPDP fiber link. One fiber is a transmit channel and the other is a receive channel. Red tape indicators have been added to the front panels and cables to aid in the proper connection of the cables (red should connect to red). A Class 1 laser is used for the light source with a power rating that is safe for unshielded human eyes.

The Fiber Out (to Pixel Server) side of the link is used to pass digitized array readout data to the Pixel Server platform.

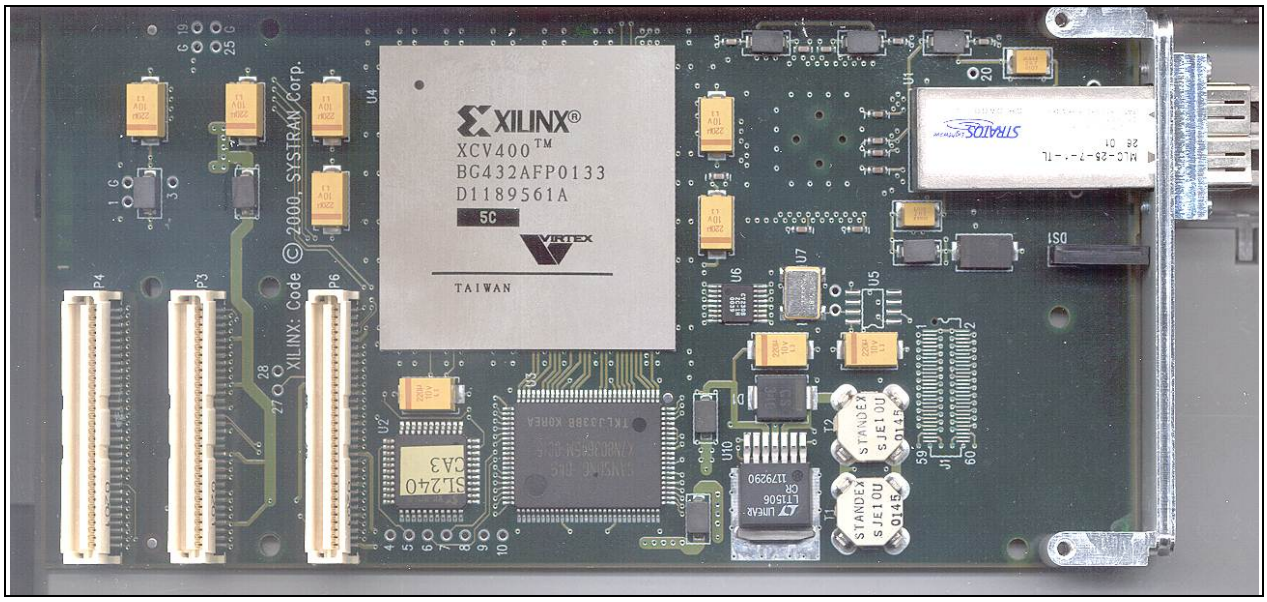

Figure 6 Photo: Systran SL240 CMC Board

3.2 Clocker

The Clocker is an embedded PowerPC + FPGA board, the IPEngine1 from Brightstar Engineering, which is used to provide communication and control of the array clocking function. The IPEngine1 has a 48MHz PowerPC CPU which runs an ELINUX operating system. Communications with outboard systems is carried over a TCP/IP 10BT Ethernet interface coupled on board to fiber media, called Clocker ENET.

An image of the operating system is decompressed from onboard FLASH memory into the 1Mx16bit DRAM. A block diagram of the IPEngine1 is provided in Figure 7.

The real time task of clocking the array patterns is done with the onboard Altera EP6016 16,000 gate FPGA. The Instrument Controller writes a Clock Table to the Clocker IPEngine's 128K x 16 bit Synchronous SRAM via the Clocker ENET link. A compiled VHDL program is loaded into the FPGA which reads out the contents of the 128kx16 bit Synchronous SRAM and executes the encoded in the Clock Table. For more information on the Clock Table see Section 3.2.2.

Software writes to the Clocker to arm it to begin clocking. Once the Clocker has been armed, it waits for the TTL Trigger from the facility to assert. Once the TTL Trigger is asserted, the Clocker begins driving array clocking signals on the Clock Control Bus.

The round trip response time for a command/PIO/acknowledge has been measured to be in the 2 to 8msec range. This is the time for a command issued by the Instrument Controller to be transmitted through the 10BT Ethernet link to the PowerPC, simple PIO operation executed and acknowledged back through the 10BT link.

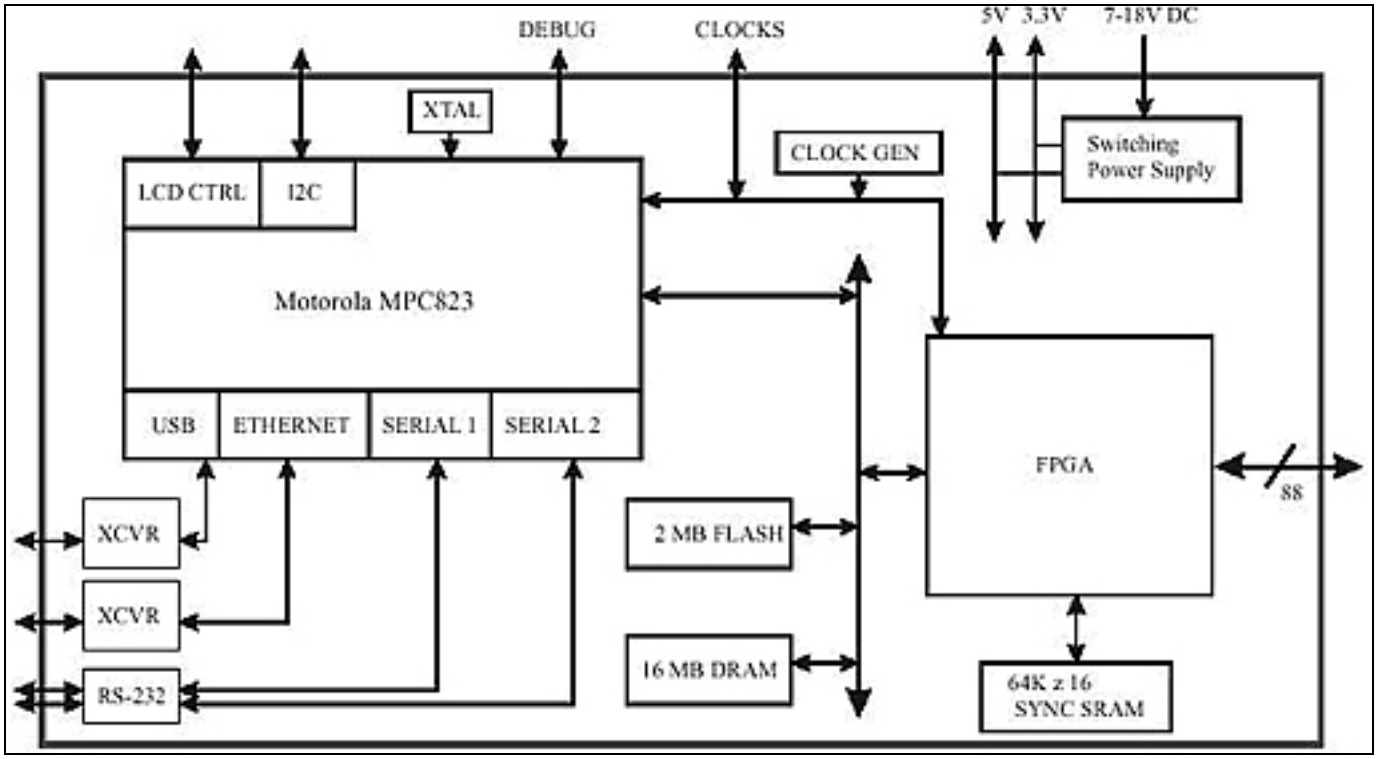

Figure 7 Block Diagram of IPEngine1

3.2.1 IPEngine1 Memory Map

A complete memory map for the IPEngine1 can be found in the attached user manual, the following is a partial list of important memory addresses:

PPC Memory Location	Description	Function	Meanings	R/W
0XFC00.0000	IA Register (IA15..IA0)	Control Register for FPGA		Write only
	Bit 0 = IA0 = patters Bits 15-8 = CNTL	Controls clock pattern generator and CONTROL BUS interface (upper 8 bits)	0 = stop pattern generator, control under PPC. 1 = ARM TRIGGER of pattern generator	
0XFC00.0002	IA Register (IA31..IA16)			Write only
0XFC00.0004	TBD	TBD	TBD	Write only
0XFC00.0006	STB Register (7-0)	STROBE outputs to bus latches		Write only
0XFC00.0008	CMDATA Register (15-0)	Command sequence DATA register (DAC programming)	Actual data written to CLKBIAS DACs	Write only
0XFC00.001C	Loop back Register (15-0)	Loops back written data		Read/Write
0XFC00.0016	COADD Register (15-0)	#COADDS = 0 to 65536		Write only
0XFC00.0018	ITIME Register (15-0)	28 bit Integration time value X 25usec, (lower bits)		Write only

PPC Memory Location	Description	Function	Meanings	R/W
0XFC00.001A	ITIME Register (27-16)	28 bit Integration time value X 25usec, (higher bits)		Write only
0XFC04.000 – FC07.FFF	256KB SSRAM	RLL Clock Pattern memory		Read/Write

Figure 8 Partial Memory Map of Clocker IPEngine1

Some notes on the Clicker's memory map:

1. SSRAM address space 0xFC04 0000
2. FPGA base address 0xFC00 0000
3. The INTEGRATION TIMER FPGA register address 0xFC00 0018
4. The ARM TRIGGER FPGA register address 0xFC00 0000

3.2.2 Clock Table Concepts

The Clock Table is a table of clocking entries. This table is read by the Clicker's FPGA to determine the sequence of clocks to be driven to the array. This section explains how to build the clock table.

A typical array readout would involve the following conceptual stages:

- Pedestal Phase:
  - A Pre-readout phase, where readout is defined as clocking out the array to be sampled.
    - During the pre-readout phase the array is typically reset to set a known charge state in the array pixels.
    - There is a time period before the next phase is started
  - A Pedestal Readout where the part of or the entire array is sequentially clocked to output analog voltages to be digitized by the cryostat mounted electronics system.
    - The array may be read a multiple number of times for Non Destructive Reads.
- An Integration Phase:
  - The clocks are held in a fixed state and charge is integrated on each pixel.
- A Signal Readout Phase:
  - Part of or the entire array is sequentially clocked to output analog voltages to be digitized by the cryostat mounted electronics system.
  - The array may be readout a multiple number of times for Non Destructive Reads.

The entries into the clocking table for the Pedestal Phase, Integration Phase, and Signal Readout Phase are qualitatively described in the following sections. The Clocking Table is illustrated in Section 3.2.2.4.

3.2.2.1 Pedestal Phase

The Pedestal Phase generally consists of a Reset Frame (ie: Pre-readout Phase) followed by a Pedestal Readout.

Reset Frame

- A FRAME ENTRY START would begin the table.
- A FRAME COUNT entry must follow with the PEDESTAL bit set. The count (run length) would indicate the number of times the this frame would be repeated. This 1st frame would typically be a RESET frame.
    - The 1st ROW COUNT entry must follow. The count (run length) would indicate the number of times the this row would be repeated.
        - The 1st PATTERN COUNT for the 1st ROW must follow. The count (run length) would indicate the number of times the following PATTERN entry would be extended beyond a single time tick of 145.833nsec (each extension is 20.833 nsec). This sets the duration of the PATTERN. The FRAME ON, ROW ON and PEDESTAL FRAME bits would be set.
        - The 1st PATTERN entry must follow. This is the actual bit pattern to be output to the Clock/Control Bus.
        - The 2nd PATTERN COUNT for the 1st ROW could follow. The FRAME ON, ROW ON and PEDESTAL FRAME bits would be set.
        - The 2nd PATTERN entry must follow.
        - Other pattern count+ pattern entries could follow.
        - The nth PATTERN COUNT for the 1st ROW would follow. The FRAME ON and PEDESTAL FRAME bits would be set, but the ROW ON would be unset to indicate the END OF ROW.
        - The nth PATTERN entry must follow.
    - An END OF ROW SPACE entry must follow to allow the FPGA pipeline to load the next entries correctly.
    - The 2nd ROW COUNT entry could follow. The count (run length) would indicate the number of times the this row would be repeated.
        - The 1st PATTERN COUNT for the 2nd ROW must follow. The FRAME ON, ROW ON and PEDESTAL FRAME bits would be set.
        - The 1st PATTERN entry must follow.
        - Other pattern count+ pattern entries could follow.
        - The nth PATTERN COUNT for the 2nd ROW would follow. The FRAME ON, PEDESTAL FRAME, ROW ON would be unset to indicate the END OF ROW and END OF FRAME.
        - The nth PATTERN entry must follow.

Pedestal Readout

- A 2nd FRAME ENTRY START could begin the table.
- A FRAME COUNT entry must follow with the PEDESTAL bit set.
    - The 1st ROW COUNT entry must follow.
        - The 1st PATTERN COUNT for the 1st ROW must follow. The FRAME ON, ROW ON and PEDESTAL FRAME bits would be set.
            - The 1st PATTERN entry must follow.
        - Other pattern count+ pattern entries could follow.
        - The nth PATTERN COUNT for the 1st ROW would follow. The FRAME ON and PEDESTAL FRAME bits would be set, but the ROW ON would be unset to indicate the END OF ROW
        - The nth PATTERN entry must follow.
    - An END OF ROW SPACE entry must follow to allow the FPGA pipeline to load the next entries correctly.
    - The 2nd ROW COUNT entry could follow. The count (run length) would indicate the number of times the this row would be repeated.
        - The 1st PATTERN COUNT for the 2nd ROW must follow. The FRAME ON, ROW ON and PEDESTAL FRAME bits would be set.
        - The 1st PATTERN entry must follow.
        - Other pattern count+ pattern entries could follow.
        - The nth PATTERN COUNT for the 2nd ROW would follow. The FRAME ON, PEDESTAL FRAME, ROW ON would be unset to indicate the END OF ROW and END OF FRAME
        - The nth PATTERN entry must follow..

3.2.2.2 Integration Phase

During an Integration Phase, the array clocks are held in a fixed state and charge is integrated on each pixel.

Integration Phase

- The END OF FRAME bit indication (set at the end of the Pedestal Phase) would start the countdown of the INTEGRATION TIMER. During this time, the FPGA waits for the counter to clear zero before proceeding.
- An END OF FRAME SPACE entry must follow to allow the FPGA pipeline to load the next entries correctly.

3.2.2.3 Signal Readout Phase

The Signal Readout Phase consists of the following Clocking Table entries.

Signal Readout Phase

- A FRAME ENTRY START would begin the table.
- A FRAME COUNT entry must follow with the PEDESTAL bit unset indicating a SIGNAL frame count.
  - The 1st ROW COUNT entry must follow.
    - The 1st PATTERN COUNT for the 1st ROW must follow. The FRAME ON, ROW ON bits would be set and the and PEDESTAL FRAME bit would be unset.
    - The 1st PATTERN entry must follow.
    - Other pattern count+ pattern entries could follow.
    - The nth PATTERN COUNT for the 1st ROW would follow. The FRAME ON bit would be set, the PEDESTAL FRAME and ROW ON (to indicate the END OF ROW) would be unset.
    - The nth PATTERN entry must follow.
  - An END OF ROW SPACE entry must follow to allow the FPGA pipeline to load the next entries correctly.
  - The 2nd ROW COUNT entry could follow.
    - The 1st PATTERN COUNT for the 2nd ROW must follow. The FRAME ON, ROW ON bits would be set and the and PEDESTAL FRAME bit would be unset.
    - The 1st PATTERN entry must follow.
    - Other pattern count+ pattern entries could follow.
    - The nth PATTERN COUNT for the 2nd ROW would follow. The FRAME ON, PEDESTAL FRAME, ROW ON would be unset to indicate the END OF ROW and END OF FRAME.
    - The nth PATTERN entry must follow.
- An END OF FRAME SPACE entry must follow to allow the FPGA pipeline to clear.
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- An END OF FRAME SPACE entry must follow to allow the FPGA pipeline to clear.

3.2.2.4 Clock Table Entries' Detailed Information

Type	SSRAM Address	Sequence Name	Typical value(s)	D15	D14	D13	D12	D11	D10	D9-0	Note
Pedestal Start	0x0000	Frame Entry Start	0x1000	0	0	0	1	0	0	000	Starts table
Pedestal Frame count	0x0001	Frame Count	0x2000	0	0	1= Pedestal Frame	0	0	0	# Frame repetitions (0 to 1023)	0=1 rep 1023=1024 reps
Pedestal 1st row count	0x0002	Row Count	0x0200	0	0	0	0	0	0	# Row repetitions (0 to 1023)	0=1 rep 1023=1024 reps
Pedestal 1st pattern count	0x0003	Pattern Count	0xE001	1 = frame_on	1 = row_on	1= Pedestal Frame	0	0	0	# Pat repetitions (0 to 1023)	0=0 rep 1023=1023 reps
Pedestal 1st pattern	0x0004	Pattern	0x0001	Clock Bit15	Clock Bit14	Clock Bit13	Clock Bit12	Clock Bit11	Clock Bit10	Clock Bits 9-0	
Pedestal 2nd pattern count	0x0005	Pattern Count	0xE002	1 = frame_on	1 = row_on	1= Pedestal Frame	0	0	0	# Pat repetitions (0 to 1023)	0=0 rep 1023=1023 reps
Pedestal 2nd pattern	0x0006	Pattern	0x0002	Clock Bit15	Clock Bit14	Clock Bit13	Clock Bit12	Clock Bit11	Clock Bit10	Clock Bits 9-0	

Type	SSRAM Address	Sequence Name	Typical value(s)	D15	D14	D13	D12	D11	D10	D9-0	Note
Pedestal 3rd pattern count	0x0005	Pattern Count	0xA004	1 = frame_on	0 = end of row	1= Pedestal Frame	0	0	0	# Pat repetitions (0 to 1023)	0=0 rep 1023=1023 reps
Pedestal 3rd pattern	0x0006	Pattern	0x0004	Clock Bit15	Clock Bit14	Clock Bit13	Clock Bit12	Clock Bit11	Clock Bit10	Clock Bits 9-0	
Pedestal End of row	0x0007	End of Row space	0x0000	0	0	0	0	0	0	000	Dummy space
Pedestal 2nd row count	0x0008	Row Count	0x0000	0	0	0	0	0	0	# Row repetitions (0 to 1023)	0=1 rep 1023=1024 reps
Pedestal Row2 1st pattern count	0x0009	Pattern Count	0x0001	0 = end of frame	0 = end of row	0= end of pedestal	0	0	0	# Pat repetitions (0 to 1023)	0=0 rep 1023=1023 reps
Pedestal Row2 1st pattern	0x000A	Pattern	0x0005	Clock Bit15	Clock Bit14	Clock Bit13	Clock Bit12	Clock Bit11	Clock Bit10	Clock Bits 9-0	
End of Pedestal, End of Row, Start Integration	0x000B	End of Frame space	0x0000	0	0	0	0	0	0	000	Dummy space, Integration timer counts down here
Signal Frame start	0x000C	Frame Entry Start	0x1000	0	0	0	1	0	0	000	Starts table
Signal Frame Count	0x000D	Frame Count	0x0000	0	0	0= Signal Frame	0	0	0	# Frame repetitions (0 to 1023)	0=1 rep 1023=1024 reps
Signal 1st row count	0x000E	Row Count	0x0000	0	0	0	0	0	0	# Row repetitions (0 to 1023)	0=1 rep 1023=1024 reps
Signal 1st pat count	0x000F	Pattern Count	0xC001	1 = frame_on	1 = row_on	0= Signal Frame	0	0	0	# Pat repetitions (0 to 1023)	0=0 rep 1023=1023 reps
Signal 1st pattern	0x0010	Pattern	0x900F	Clock Bit15	Clock Bit14	Clock Bit13	Clock Bit12	Clock Bit11	Clock Bit10	Clock Bits 9-0	
Signal 2nd pattern count	0x0011	Pattern Count	0x0000	0 = end of frame	0 = end of row	0= end of signal	0	0	0	# Pat repetitions (0 to 1023)	0=0 rep 1023=1023 reps
Signal 2nd pattern	0x0012	Pattern	0x0000	Clock Bit15	Clock Bit14	Clock Bit13	Clock Bit12	Clock Bit11	Clock Bit10	Clock Bits 9-0	
End of Signal, End of Row, Restart	0x0013	End of Frame space	0x0000	0	0	0	0	0	0	000	Dummy space, clocker starts at 0x0000
End of Signal, End of Row, Restart	0x0013	End of Frame space	0x0000	0	0	0	0	0	0	000	Dummy space, clocker starts at 0x0000
End of Signal, End of Row, Restart	0x0013	End of Frame space	0x0000	0	0	0	0	0	0	000	Dummy space, clocker starts at 0x0000

3.3 Catcher

The Catcher is an embedded PowerPC + FPGA board, the IPEngine1 from Brightstar Engineering, which is used to buffer the digital array data as it is received from the Read Data Bus. The Catcher takes two 16 bit data streams from the Read Data Bus and buffers it into the XMT Buffer. The buffer size is optimized for throughput on the Frame Data Bus. When the buffer is full, the Clocker signals the SL240 to transmit the contents of the buffer.

The IPengine1 has a 48MHz PowerPC CPU which runs an ELINUX operating system. Communications with outboard systems is carried over a TCP/IP 10BT Ethernet interface coupled on board to fiber media, called Catcher ENET. The FPGA image of the Clocker is received via the Catcher ENET link at power up.

An image of the operating system is decompressed from onboard FLASH memory into the 1Mx16bit DRAM. A block diagram of the IPEngine1 is provided in Figure 7. A partial memory map of the IPEngine1 is provided in Figure 8.

4 Configuration and Settings

This section specifies the configuration and settings options of the FCRYO2. **Generally the customer should not have to modify any of these settings. This information is provided for informational and development purposes.**

4.1 Motherboard CPLD Firmware Configuration

There are 3 Cypress CY37512P208-125 CPLDs on the motherboard, U4, U5, and U31. U4 interfaces the Clock IPEngine FPGA to the backplane Clock Bus. U5 handles the interfacing of pixel data into the dual port ram. U31 is unprogrammed and tristated. The CPLDs are programmed using Cypress Semiconductor JTAG hardware plugged into each chips respective JTAG 10 pin header .

U4 CPLD: Filename = FCRYO_clock.jed, Checksum CBF07, release level 1.0, JTAG header = JP4.
U5 CPLD: Filename = FCRYO_pixeldata.jed, Checksum CA9F9, release level 1.0, JTAG header = JP4.
U31 CPLD: Filename = NONE, release level NONE, JTAG header = JP9.

4.2 SL240 Configuration

The S1 switch on the SL240 CMC controls several settings for the SL240 CMC board. For a more detailed explanation refer to the Systran documentation. Note the PCB has on board pull-up resistors so an OFF switch setting will input a +5V ='1' signal and an ON setting will input a 0V='0'. A table of the S1 settings is provided in Figure 9.

The FCRYO2 is shipped with the S1 switch properly configured. **The customer should not have to modify any of the settings of the S1 switch.**

Signal Name	S1 switch	Position	Setting	Note
CRC_EN	1	OFF	CRC checking enabled	CRC checksum
CLK_C0	2	ON	62.5Mhz	CLK_CFG0&1, FPDP-TM clock configuration
CLK_C1	3	ON	62.5Mhz	
IGNOREFC	4	ON	Flow control enabled	Ignore Flow Control 1= ignore, 0=enable
C_SYNC	5	ON	Per manual	Convert Sync "set to '0' for all FPDP operations".
TNRDY_N	6	OFF	FPDP ready	Transmit Not Ready " set to '1' to tell the FPDP interface that the FPDP receiver is ready to accept data."
TSUS_N	7	OFF	Enable transmit	Transmit Suspend "Otherwise set to '1'"
No function	8	Don't care	Nothing	No function

Figure 9 SL240 CMC S1 Switch Settings

4.3 IPEngine1 Configuration

Both the Clocker IPEngine1 and the Catcher IPEngine1 have some configuration options. The on board power supplies can be disabled. The embedded FPGA must be loaded with an FPGA image each time the system is powered up.

The customer should not modify any hardware configuration of the Clocker IPEngine. This information is only included for informational purposes.

4.3.1 Power Supplies

The customer should not modify any hardware configuration of the Clocker IPEngine.

There are 2 user settable jumpers on the IPEngine1 PCB. There are 4 pins on jumper JP1. Installing a shunt between pins 3 and 4 disables both the on board +5V and +3.3V power supplies. Installing a shunt between pins 1 and 2 disables only the on board +5V power supply. The FCRYO2's IPEngine1 ships with both on board power supplies disabled. These jumpers are shown in the photo in Figure 10.

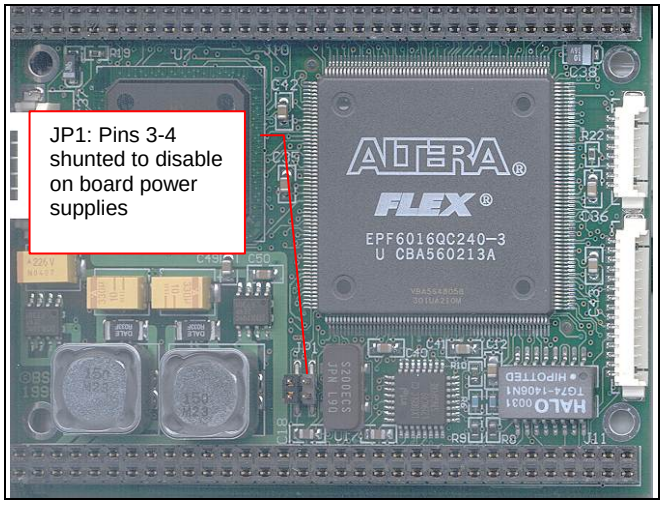

Figure 10 Photo: IPEngine1 Configuration

4.3.2 FPGA Firmware Configuration

The customer should not have to modify any hardware configuration of the Clocker IPEngine.

Each IPEngine has an Altera FPGA that needs to be programmed. Brightstar software makes it possible to program the FPGA over the network. The file format is a .rbf (Altera raw binary format). The FPGA configuration is volatile and is reprogrammed each time the system is powered up.

The FCRYO2's current FPGA images are contained in the following files:

- Clock FPGA: Filename = sample2_jitter.rbf, release level 1.0
- Pixel FPGA: Filename = pixel_ipengine_more_syncs.rbf, release level 1.0.

5 I/O

This section defines the Inputs and Outputs of the FCRYO2 board. All of the FCRYO2's I/O are via 2 backplane connectors. Each connector has 3 columns of 32 pins. The left column of pins is column C, the middle B, the right A. The top connector is referred to as P1 and the bottom is referred to as P2. The P1 portion of the backplane is implemented as the P2 connections are defined in the VME standard, not as P1 is defined in the VME standard. Both the P1 and P2 connectors have shared B column pins that connect to a bus with standard termination. The A and C column pins are custom defined.

WARNING: **The FCRYO2 board is not compatible with the VME standard**, though it may appear to be. Inserting the FCRYO2 in a standard VME chassis will likely cause a catastrophic failure. Likewise inserting standard VME cards into the chassis is prohibited and extremely risky.

Clock Control Bus: The Clock Control Bus is a digital output of the FCRYO2 to the backplane P2 connector. There are 3 parts of the bus. The Clock Control Bus drives CLKBIAS boards. The CB_D[15:0] signals control the CLKBIAS' analog output switches. The bus also contains control signals CB_CW[7:0] which are used to select and program specific CLKBIAS DAC circuits. CB_WR! controls latching of the Clock Control Bus by the CLKBIAS board. Identical Clock Control Bus signals are driven out of the FCRYO2 on 2 columns of the P2 connector, one on the B column, one on the C column.

Read Data Bus: The Read Data Bus delivers digital array readout data to the FCRYO2. There are two Read Data Buses on the backplane that each deliver 16 bit data streams. The RB_D[15:0] input signals are the data portion of the bus.

5.1 P1 Connector Pinout

The "I/O/Bi" column indicates whether the signal is an Input (I), Output (O), or Bidirectional (Bi). This column also indicates whether the signal is a Digital (D), Analog (A), or a Power (PWR) signal.

Col. C Pins	Signal	I/O/Bi	Col. B Pins	Signal	I/O/Bi	Col. A Pins	Signal	I/O/Bi
P1 C1	*Unused*	-	P1 B1	+5V	PWR	P1 A1	+15V	PWR
P1 C2	*Unused*	-	P1 B2	DGND	PWR	P1 A2	AGND	PWR
P1 C3	RB_RD!	D O	P1 B3	RB_RD!	D O	P1 A3	*Unused*	-
P1 C4	RB_D0	D I	P1 B4	RB_D0	D I	P1 A4	*Unused*	-
P1 C5	RB_D1	D I	P1 B5	RB_D1	D I	P1 A5	*Unused*	-
P1 C6	RB_D2	D I	P1 B6	RB_D2	D I	P1 A6	*Unused*	-
P1 C7	RB_D3	D I	P1 B7	RB_D3	D I	P1 A7	*Unused*	-
P1 C8	RB_D4	D I	P1 B8	RB_D4	D I	P1 A8	*Unused*	-
P1 C9	RB_D5	D I	P1 B9	RB_D5	D I	P1 A9	*Unused*	-
P1 C10	RB_D6	D I	P1 B10	RB_D6	D I	P1 A10	*Unused*	-
P1 C11	RB_D7	D I	P1 B11	RB_D7	D I	P1 A11	*Unused*	-
P1 C12	*Unused*	-	P1 B12	DGND	PWR	P1 A12	AGND	PWR
P1 C13	*Unused*	-	P1 B13	+5V	PWR	P1 A13	*Unused*	-
P1 C14	RB_D8	D I	P1 B14	RB_D8	D I	P1 A14	*Unused*	-
P1 C15	RB_D9	D I	P1 B15	RB_D9	D I	P1 A15	*Unused*	-
P1 C16	RB_D10	D I	P1 B16	RB_D10	D I	P1 A16	*Unused*	-
P1 C17	RB_D11	D I	P1 B17	RB_D11	D I	P1 A17	*Unused*	-
P1 C18	RB_D12	D I	P1 B18	RB_D12	D I	P1 A18	*Unused*	-
P1 C19	RB_D13	D I	P1 B19	RB_D13	D I	P1 A19	*Unused*	-
P1 C20	RB_D14	D I	P1 B20	RB_D14	D I	P1 A20	*Unused*	-
P1 C21	RB_D15	D I	P1 B21	RB_D15	D I	P1 A21	*Unused*	-
P1 C22	*Unused*	-	P1 B22	DGND	PWR	P1 A22	AGND	PWR
P1 C23	RB_SD0	D I	P1 B23	RB_SD0	D I	P1 A23	*Unused*	-
P1 C24	RB_SD1	D I	P1 B24	RB_SD1	D I	P1 A24	*Unused*	-
P1 C25	RB_SD2	D I	P1 B25	RB_SD2	D I	P1 A25	*Unused*	-
P1 C26	RB_SD3	D I	P1 B26	RB_SD3	D I	P1 A26	*Unused*	-
P1 C27	RB_SD4	D I	P1 B27	RB_SD4	D I	P1 A27	*Unused*	-
P1 C28	RB_SD5	D I	P1 B28	RB_SD5	D I	P1 A28	*Unused*	-
P1 C29	RB_SD6	D I	P1 B29	RB_SD6	D I	P1 A29	*Unused*	-
P1 C30	RB_SD7	D I	P1 B30	RB_SD7	D I	P1 A30	*Unused*	-
P1 C31	*Unused*	-	P1 B31	DGND	PWR	P1 A31	*AGND*	PWR
P1 C32	*Unused*	-	P1 B32	+5V	PWR	P1 A32	-15V	PWR

5.2 P2 Connector Pinout

The "I/O/Bi" column indicates whether the signal is an Input (I), Output (O), or Bidirectional (Bi). This column also indicates whether the signal is a Digital (D), Analog (A), or a Power (PWR) signal.

Col. C Pins	Signal	I/O/Bi	Col. B Pins	Signal	I/O/Bi	Col. A Pins	Signal	I/O/Bi
P2 C1	*Unused*	-	P2 B1	+5V	PWR	P2 A1	+15V	PWR
P2 C2	*Unused*	-	P2 B2	DGND	PWR	P2 A2	AGND	PWR
P2 C3	CB_WR!	D O	P2 B3	CB_WR!	D O	P2 A3	*Unused*	-
P2 C4	CB_D0	D O	P2 B4	CB_D0	D O	P2 A4	*Unused*	-
P2 C5	CB_D1	D O	P2 B5	CB_D1	D O	P2 A5	*Unused*	-
P2 C6	CB_D2	D O	P2 B6	CB_D2	D O	P2 A6	*Unused*	-
P2 C7	CB_D3	D O	P2 B7	CB_D3	D O	P2 A7	*Unused*	-
P2 C8	CB_D4	D O	P2 B8	CB_D4	D O	P2 A8	*Unused*	-
P2 C9	CB_D5	D O	P2 B9	CB_D5	D O	P2 A9	*Unused*	-
P2 C10	CB_D6	D O	P2 B10	CB_D6	D O	P2 A10	*Unused*	-
P2 C11	CB_D7	D O	P2 B11	CB_D7	D O	P2 A11	*Unused*	-
P2 C12	*Unused*	-	P2 B12	DGND	PWR	P2 A12	AGND	PWR
P2 C13	*Unused*	-	P2 B13	+5V	PWR	P2 A13	*Unused*	-
P2 C14	CB_D8	D O	P2 B14	CB_D8	D O	P2 A14	*Unused*	-
P2 C15	CB_D9	D O	P2 B15	CB_D9	D O	P2 A15	*Unused*	-
P2 C16	CB_D10	D O	P2 B16	CB_D10	D O	P2 A16	*Unused*	-
P2 C17	CB_D11	D O	P2 B17	CB_D11	D O	P2 A17	*Unused*	-
P2 C18	CB_D12	D O	P2 B18	CB_D12	D O	P2 A18	*Unused*	-
P2 C19	CB_D13	D O	P2 B19	CB_D13	D O	P2 A19	*Unused*	-
P2 C20	CB_D14	D O	P2 B20	CB_D14	D O	P2 A20	*Unused*	-
P2 C21	CB_D15	D O	P2 B21	CB_D15	D O	P2 A21	*Unused*	-
P2 C22	*Unused*	-	P2 B22	DGND	PWR	P2 A22	AGND	PWR
P2 C23	CB_CW0	D O	P2 B23	CB_CW0	D O	P2 A23	*Unused*	-
P2 C24	CB_CW1	D O	P2 B24	CB_CW1	D O	P2 A24	*Unused*	-
P2 C25	CB_CW2	D O	P2 B25	CB_CW2	D O	P2 A25	*Unused*	-
P2 C26	CB_CW3	D O	P2 B26	CB_CW3	D O	P2 A26	*Unused*	-
P2 C27	CB_CW4	D O	P2 B27	CB_CW4	D O	P2 A27	*Unused*	-
P2 C28	CB_CW5	D O	P2 B28	CB_CW5	D O	P2 A28	*Unused*	-
P2 C29	CB_CW6	D O	P2 B29	CB_CW6	D O	P2 A29	*Unused*	-
P2 C30	CB_CW7	D O	P2 B30	CB_CW7	D O	P2 A30	*Unused*	-
P2 C31	*Unused*	-	P2 B31	DGND	PWR	P2 A31	AGND	PWR
P2 C32	*Unused*	-	P2 B32	+5V	PWR	P2 A32	-15V	PWR

6 Acronyms and Definitions

CPLD	Complex Programmable Logic Device
CS	Chip Select
DAC	Digital to Analog Converter
DSP	Digital Signal Processor
FPGA	Field Programmable Gate Array
SSRAM	Synchronous SRAM