Mauna Kea Infrared
PREAMP8
8 Channel Differential Input, Array Optimized Low Noise Preamplifier Board

MKIR# 700-158-01
Rev 1.5
Last Modified 10/19/04

WARNING: **The PREAMP8 board is not compatible with the VME standard**, though it may appear to be. Inserting the PREAMP8 in a standard VME chassis will likely cause a **catastrophic failure**. Likewise inserting standard VME cards into the chassis is prohibited and extremely risky.

Revision History

Revision	Author	Summary of revisions	Date
1.5	Mike Thompson	Initial release to customer.	10/19/04
1.0	Peter Onaka	Initial Revision	11/17/99

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1 PREAMP8 Overview

The PREAMP8 is an 8 channel differential input preamplifier with independent fixed gains. Each amplifier consists of a high impedance input instrumentation amp with shared onboard offset voltage. It is intended to amplify analog array output signals. The multilayer printed circuit board construction employs multiple ground/power planes for shielding. The board is configured for specific bandwidth, load, and gain levels to match specific array requirements.

Figure 1 provides a photo of the front panel of the PREAMP8. Figure 2 provides a photo of the component side of the PREAMP8 board.

2 Technical Specifications for the PREAMP8

This section provides a quick overview of the technical features of the PREAMP8.

2.1 General Specifications

- 8 Independent Channels
- Classic 3 Opamp Instrumentation Amp Channels
- Fixed Gain (X5 for InSb 1024x1024)
- Typical Noise $\leq$ 39 nV/Hz^{-2} @ X5 gain, 1K source resistance and offset
- Typical Bandwidth 3 MHz (Raytheon 152 or 206 mux)
- Typical Rise/Fall times @ 3 MHz
- On board 12 bit DACs, Offset and Vref
- 10K Input Load Resistor or Current Source

2.2 Power Requirements

- +5V 120 mA Typ.
- +15V 480 mA Typ.
- -15V 480 mA Typ.

2.3 Mechanical Specifications

- Eurocard 6U (160mm x 233.35mm) Form Factor (*Note: the board is not electrically compatible with VME standards*)
- P1 96 pin DIN Connector, P2 DIN 41612, 96 Pin Connector
- 6 Layer PCB Construction with Internal Ground and Power Layers

Figure 1 Photo: PREAMP8 Faceplate

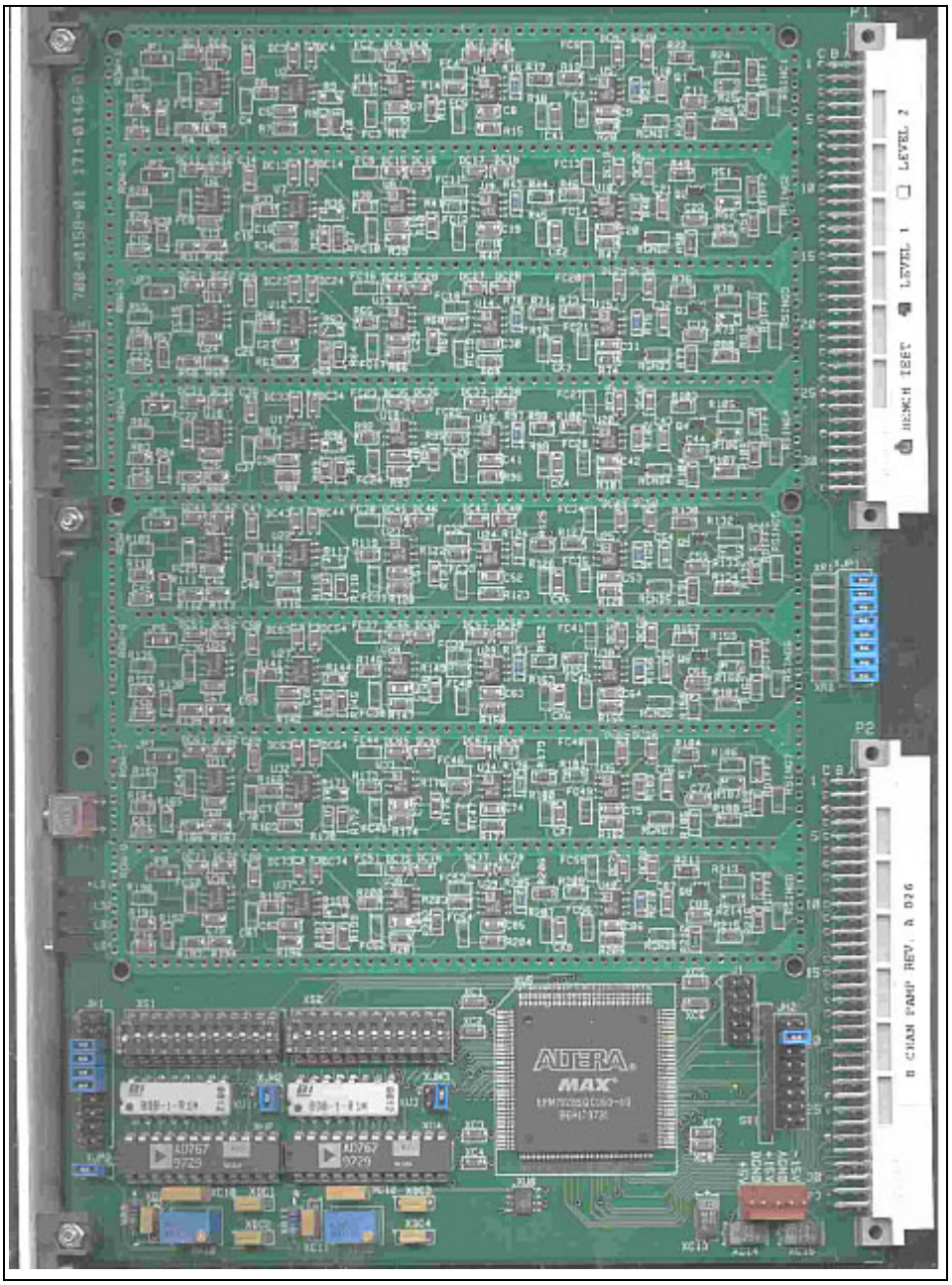


Figure 2 Photo: Component Side of PREAMP8

3 Functional Description

This section provides a functional description of the PREAMP8 board. See Figure 3 for a block diagram of the PREAMP8.

The PREAMP8 is an 8 channel differential input preamplifier with independent fixed gains (X5). Each amplifier consists of a high impedance input instrumentation amp with shared onboard offset voltage. Analog outputs and references from an array or mux are routed into the PREAMP8 on the Sig[8:1]+ and Sig[8:1]- input pins. The PREAMP8 board amplifies eight channels of analog array outputs. The amplified signals are output on the POST[8:1] signals. In an array controller implementation these amplified output signals would then be sent to ADC boards to be digitized.

The PREAMP8 boards have an offset voltage option on the inputs to the amplifiers. They are configured by an Offset DAC with 12 DIP switch positions for manually setting the offset voltage. The default setting for the Offset DAC is 0 volts, which corresponds to DIP[11] set high and DIP[10:0] set low.

The PREAMP8 boards also have a voltage reference bias voltage (VREF) option for the current source loads on the inputs to the amplifiers. They are configured by the VREF DAC with 12 DIP switch positions for manually setting the VREF. The default setting for the VREF DAC is 0 volts, which corresponds to DIP[11] set high and DIP[10:0] set low.

See Figure 3 for a block diagram of the PREAMP8.

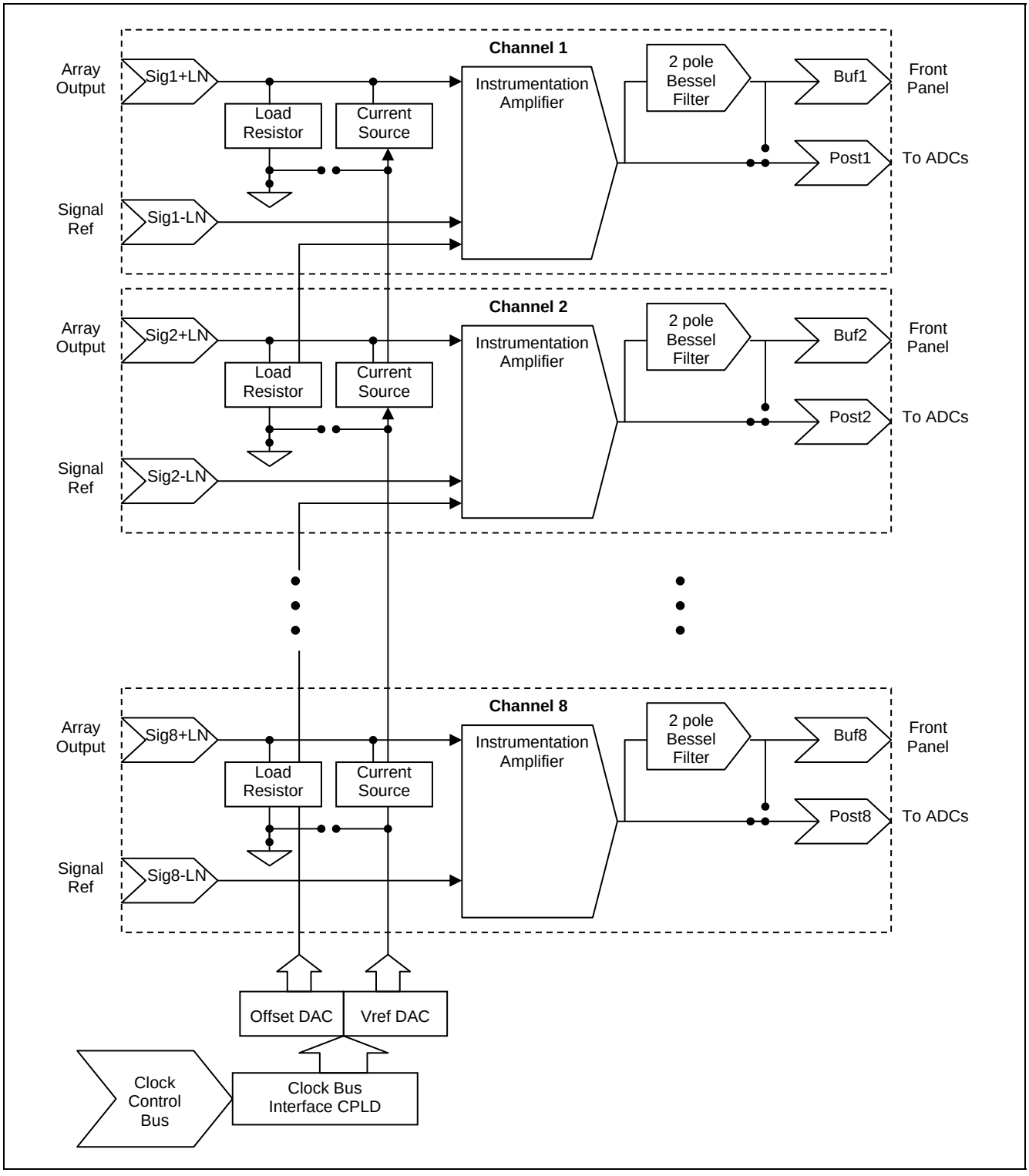


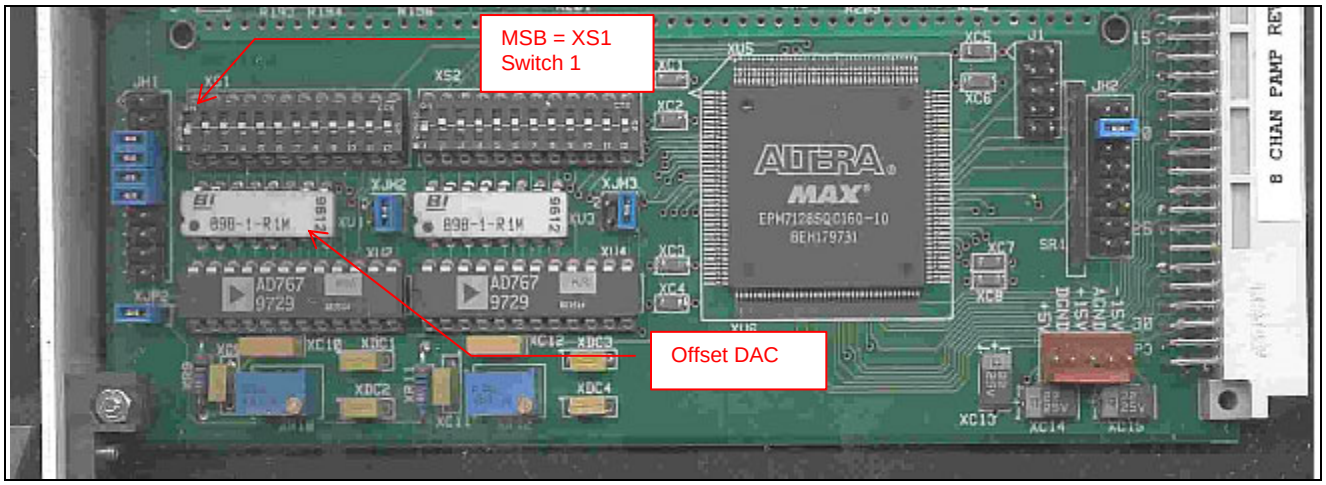
Figure 3 Block Diagram of PREAMP8

3.1 Inputs

Eight of the source follower outputs of an array are input into the PREAMP8 via the P1 connector. The schematic signal names are 'SIG#+LN' (# =1-8) and the corresponding return or reference signals are 'SIG#-LN'. Refer to Section 4 for the pin assignments on P1. For the Raytheon/SBRC 1024x1024 InSb array on the 152 or 206 mulitplexors, 1% 10K source resistances are used on the SIG#+LN inputs. An optional FET based constant current source can be implemented with a change in the SMD configuration.

3.2 Offset Voltage

A 12 bit Digital to Analog Converter (DAC), an Analog Devices AD767, provides a DIP switch (XS1) settable Offset voltage for the inputs. The default setting is for 0 volts (MSB=DAC11 high, all other bits low). Individual offsets 'OFFSET1-8' then pass through a shunt header, XJP1. Currently, the divider resistors XR1-8 are not populated (care would have to be exercised to make sure the Imax of the DAC is not exceeded).



3.3 Instrumentation Amplifier

The instrumentation amplifier configuration was chosen for its high common mode noise rejection. Each of the eight channels in the PREAMP8 are almost identically laid out and follow strict grounding and shielding design rules. The gain is fixed at X5 and the bandwidth is limited to ~2.9Mhz with resulting calculated noise (with a 1K source impedance) is equal to 53.2 uV. For the +/-2.5 V input range of the ADCs' one bit (LSB) is equal to 76 uV so the preamplifier contributes less than 1 LSB to noise.

3.4 Bessel Filter

A 2 pole Bessel filter follows the instrumentation amp. In the normal configuration, its output only feeds the front panel connectors. The Sallen-Key circuit has been set for a 3.3 Mhz low pass and a gain = 1.

3.5 VREF Voltage DAC

A 12 bit DAC circuit similar to the OFFSET DAC provides a reference bias voltage for the optional constant current source loads (at the inputs of the instrumentation amplifiers). The LSB is equal to 4.88 mV (+/- 10V range).

3.6 Board Configuration, Test Headers

This section provides details on configuring the PREAMP8 board and explains the functionality of the test headers.

3.6.1 JH2 CPLD Configuration Header

The JH2 configuration header configures the Altera MAX7128 CPLD, called the Clock Bus Interface CPLD. The CPLD is mainly used to provide a control interface for the on board DACs. Positions 1 and 2 on the header set the board address for the Offset and VREF DACs. As shown the board address for the PREAMP8 boards is:

- Position 1 = address bit 0 = 1
- Position 2 = address bit 1 = 0
- PREAMP8 board address=1

(NOTE: this does not overlap with the CLKBIAS board in the Redstar3 array controller. The SetDac command would have to be modified to allow the Control Word bits 7 and 6 to be both set in the command sequence to enable PREAMP8 DAC programming).

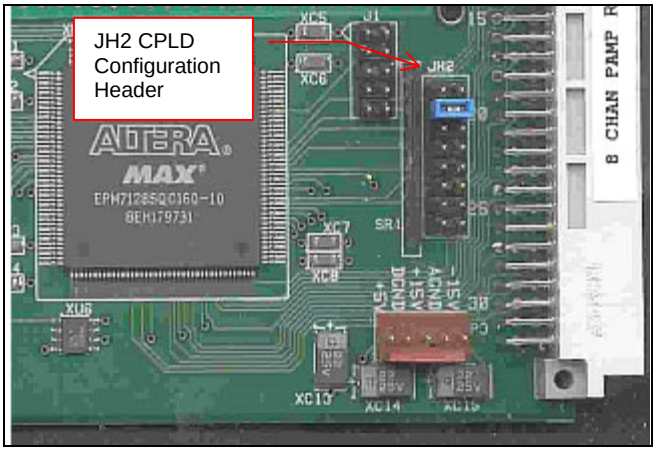


Figure 4 Photo: JH2 CPLD Configuration Header

3.6.2 Offset XS1 and VREF XS2 Dipswitch Settings

So far it has not been necessary to offset the input voltage so the standard setting has been 0 Volts. VREF is also not used since a 10K resistor is used for the array output load and is therefore set to 0 volts.

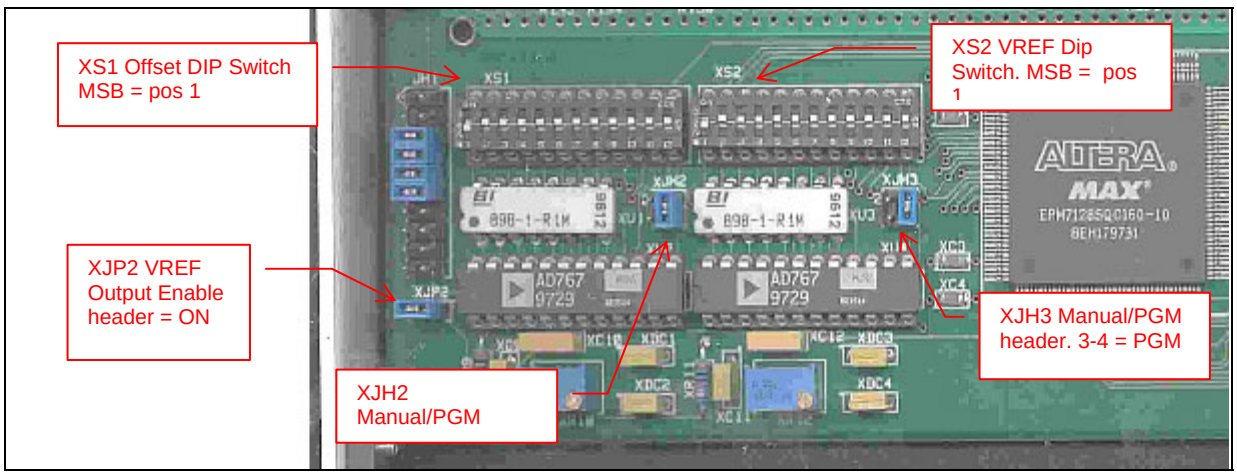


Figure 5 Photo: PREAMP8 Configuration and Test Headers

4 I/O

This section defines the Inputs and Outputs of the PREAMP8. All of the PREAMP8's I/O are via 2 backplane connectors. Each connector has 3 columns of 32 pins. The left column of pins is column C, the middle B, the right A. The top connector is referred to as P1 and the bottom is referred to as P2. The P1 portion of the backplane is implemented as the P2 connections are defined in the VME standard, not as P1 is defined in the VME standard. Both the P1 and P2 connectors have B column pins that connect to a shared bus with standard termination. The A and C column pins are custom defined.

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4.1 P1 Connector Pinout

The signals SIG[8:1]+LN and SIG[8:1]+LN are the inputs to the PREAMP8 that are to be amplified.

The "I/O/Bi" column indicates whether the signal is an Input (I), Output (O), or Bidirectional (Bi). This column also indicates whether the signal is a Digital (D), Analog (A), or a Power (PWR) signal.

Col. C Pins	Signal	I/O/Bi	Col. B Pins	Signal	I/O/Bi	Col. A Pins	Signal	I/O/Bi
P1 C1	*Unused*	-	P1 B1	*N.C.*	-	P1 A1	+15V	PWR
P1 C2	*Unused*	-	P1 B2	*N.C.*	-	P1 A2	AGND	PWR
P1 C3	SIG1+LN	A I	P1 B3	*N.C.*	-	P1 A3	SIG1-LN	A I
P1 C4	AGND	A I	P1 B4	*N.C.*	-	P1 A4	AGND	A I
P1 C5	SIG2+LN	A I	P1 B5	*N.C.*	-	P1 A5	SIG2-LN	A I
P1 C6	AGND	A I	P1 B6	*N.C.*	-	P1 A6	AGND	A I
P1 C7	SIG3+LN	A I	P1 B7	*N.C.*	-	P1 A7	SIG3-LN	A I
P1 C8	AGND	A I	P1 B8	*N.C.*	-	P1 A8	AGND	A I
P1 C9	SIG4+LN	A I	P1 B9	*N.C.*	-	P1 A9	SIG4-LN	A I
P1 C10	AGND	A I	P1 B10	*N.C.*	-	P1 A10	AGND	A I
P1 C11	SIG5+LN	A I	P1 B11	*N.C.*	-	P1 A11	SIG5-LN	A I
P1 C12	AGND	A I	P1 B12	*N.C.*	-	P1 A12	AGND	PWR
P1 C13	SIG6+LN	A I	P1 B13	*N.C.*	-	P1 A13	SIG6-LN	A I
P1 C14	AGND	A I	P1 B14	*N.C.*	-	P1 A14	AGND	A I
P1 C15	SIG7+LN	A I	P1 B15	*N.C.*	-	P1 A15	SIG7-LN	A I
P1 C16	AGND	A I	P1 B16	*N.C.*	-	P1 A16	AGND	A I
P1 C17	SIG8+LN	A I	P1 B17	*N.C.*	-	P1 A17	SIG8-LN	A I
P1 C18	AGND	A I	P1 B18	*N.C.*	-	P1 A18	AGND	A I
P1 C19	*Unused*	-	P1 B19	*N.C.*	-	P1 A19	*Unused*	-
P1 C20	*Unused*	-	P1 B20	*N.C.*	-	P1 A20	*Unused*	-
P1 C21	*Unused*	-	P1 B21	*N.C.*	-	P1 A21	*Unused*	-
P1 C22	*Unused*	-	P1 B22	*N.C.*	-	P1 A22	AGND	PWR
P1 C23	VREF+	A O	P1 B23	*N.C.*	-	P1 A23	*Unused*	-
P1 C24	OFFSET1	A O	P1 B24	*N.C.*	-	P1 A24	*Unused*	-
P1 C25	OFFSET2	A O	P1 B25	*N.C.*	-	P1 A25	*Unused*	-
P1 C26	OFFSET3	A O	P1 B26	*N.C.*	-	P1 A26	*Unused*	-
P1 C27	OFFSET4	A O	P1 B27	*N.C.*	-	P1 A27	*Unused*	-
P1 C28	OFFSET5	A O	P1 B28	*N.C.*	-	P1 A28	*Unused*	-
P1 C29	OFFSET6	A O	P1 B29	*N.C.*	-	P1 A29	*Unused*	-
P1 C30	OFFSET7	A O	P1 B30	*N.C.*	-	P1 A30	*Unused*	-
P1 C31	OFFSET8	A O	P1 B31	*N.C.*	-	P1 A31	AGND	PWR
P1 C32	VREF+	A O	P1 B32	*N.C.*	-	P1 A32	-15V	PWR

4.2 P2 Connector Pinout

The signals CB_WR!, CB_D[15:0], and CB_CW[7:0] make up the Clock Control Bus. The signals POST[8:1] are the amplified analog array readout signals and POST[8:1]RTN are their corresponding ground signals.

The "I/O/Bi" column indicates whether the signal is an Input (I), Output (O), or Bidirectional (Bi). This column also indicates whether the signal is a Digital (D), Analog (A), or a Power (PWR) signal.

Col. C Pins	Signal	I/O/Bi	Col. B Pins	Signal	I/O/Bi	Col. A Pins	Signal	I/O/Bi
P2 C1	*Unused*	-	P2 B1	+5V	PWR	P2 A1	+15V	PWR
P2 C2	AGND	A O	P2 B2	DGND	PWR	P2 A2	AGND	PWR
P2 C3	POST1	A O	P2 B3	CB_WR!	D I	P2 A3	POST1RTN	A O
P2 C4	AGND	A O	P2 B4	CB_D0	D I	P2 A4	AGND	A O
P2 C5	POST2	A O	P2 B5	CB_D1	D I	P2 A5	POST2RTN	A O
P2 C6	AGND	A O	P2 B6	CB_D2	D I	P2 A6	AGND	A O
P2 C7	POST3	A O	P2 B7	CB_D3	D I	P2 A7	POST3RTN	A O
P2 C8	AGND	A O	P2 B8	CB_D4	D I	P2 A8	AGND	A O
P2 C9	POST4	A O	P2 B9	CB_D5	D I	P2 A9	POST4RTN	A O
P2 C10	AGND	A O	P2 B10	CB_D6	D I	P2 A10	AGND	A O
P2 C11	POST5	A O	P2 B11	CB_D7	D I	P2 A11	POST5RTN	A O
P2 C12	AGND	A O	P2 B12	DGND	PWR	P2 A12	AGND	PWR
P2 C13	POST6	A O	P2 B13	+5V	PWR	P2 A13	POST6RTN	A O
P2 C14	AGND	A O	P2 B14	CB_D8	D I	P2 A14	AGND	A O
P2 C15	POST7	A O	P2 B15	CB_D9	D I	P2 A15	POST7RTN	A O
P2 C16	AGND	A O	P2 B16	CB_D10	D I	P2 A16	AGND	A O
P2 C17	POST8	A O	P2 B17	CB_D11	D I	P2 A17	POST8RTN	A O
P2 C18	AGND	A O	P2 B18	CB_D12	D I	P2 A18	AGND	A O
P2 C19	*Unused*	-	P2 B19	CB_D13	D I	P2 A19	AGND	A O
P2 C20	*Unused*	-	P2 B20	CB_D14	D I	P2 A20	*Unused*	-
P2 C21	*Unused*	-	P2 B21	CB_D15	D I	P2 A21	*Unused*	-
P2 C22	*Unused*	-	P2 B22	DGND	PWR	P2 A22	AGND	PWR
P2 C23	*Unused*	-	P2 B23	CB_CW0	D I	P2 A23	*Unused*	-
P2 C24	*Unused*	-	P2 B24	CB_CW1	D I	P2 A24	*Unused*	-
P2 C25	*Unused*	-	P2 B25	CB_CW2	D I	P2 A25	*Unused*	-
P2 C26	*Unused*	-	P2 B26	CB_CW3	D I	P2 A26	*Unused*	-
P2 C27	*Unused*	-	P2 B27	CB_CW4	D I	P2 A27	*Unused*	-
P2 C28	*Unused*	-	P2 B28	CB_CW5	D I	P2 A28	*Unused*	-
P2 C29	*Unused*	-	P2 B29	CB_CW6	D I	P2 A29	*Unused*	-
P2 C30	*Unused*	-	P2 B30	CB_CW7	D I	P2 A30	*Unused*	-
P2 C31	*Unused*	-	P2 B31	DGND	PWR	P2 A31	AGND	PWR
P2 C32	*Unused*	-	P2 B32	+5V	PWR	P2 A32	-15V	PWR

5 Acronyms and Definitions

ADC	Analog to Digital Converter
AGND	Analog Ground
DGND	Digital Ground
GND	Electrical ground
LSB	Least Significant Bit
MKIR	Mauna Kea Infrared
MSB	Most Significant Bit
PCB	Printed Circuit Board