Mauna Kea Infrared
ADC8
8 Channel 2 MHz 16 bit Analog to Digital Converter Board

MKIR# 700-155-01
Rev 1.6
Last Modified 10/19/04

WARNING: **The ADC8 board is not compatible with the VME standard**, though it may appear to be. Inserting the ADC8 in a standard VME chassis will likely cause a catastrophic failure. Likewise inserting standard VME cards into the chassis is prohibited and extremely risky.

Revision History

Revision	Author	Summary of revisions	Date
1.6	Mike Thompson	Release to customer.	10/19/04
1.0	Peter Onaka	Initial Revision	10/27/99

Table of Contents

Table of Figures and Photos

1 ADC8 Overview

The ADC8 is an 8 channel differential input Analog to Digital Converter board. The primary function of the ADC8 is to convert preamplified analog array outputs to digital format. Each channel uses an Analogic 2MHz 16 bit ADC4322 analog to digital converter. The multilayer printed circuit board construction employs multiple ground/power planes for shielding.

Figure 1 provides a photo of the front panel of the ADC8. Figure 2 provides a photo of the component side of the ADC8 board.

2 Technical Specifications for the ADC8

This section provides a quick overview of the technical features of the ADC8.

2.1 General Specifications

- 8 Independent Channels
- 8 Analogic ADC4322s
- Altera MAX7128 CPLD
- Input range settings (+/-2.5V,+/-5.0V,0-10V)
- 6 layer PCB

2.2 Power Requirements

- +5V 696 mA Typ.
- +15V 568 mA Typ.
- -15V 488 mA Typ.

2.3 Mechanical Specifications

- Eurocard 6U (160mm x 233.35mm) Form Factor
- P1 96 pin DIN Connector, P2 DIN 41612, 96 Pin Connector
- 6 Layer PCB Construction with Internal Ground and Power Layers

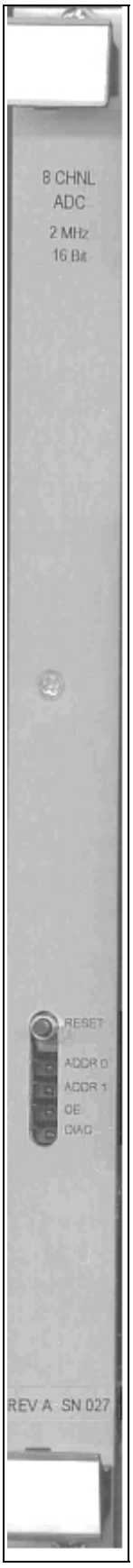

Figure 1 Photo: ADC8 Faceplate

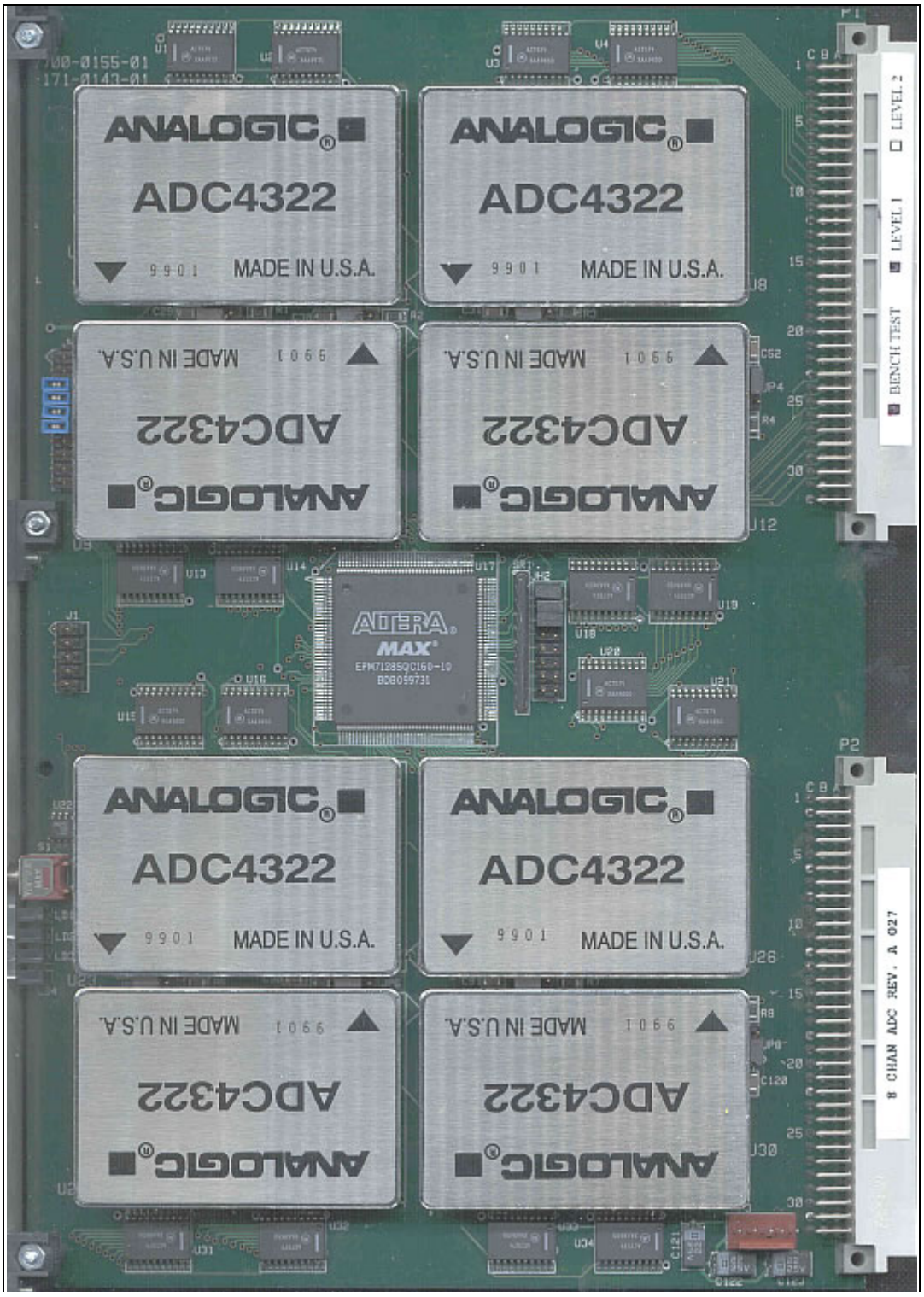

Figure 2 Photo: Component Side of ADC8

3 Functional Description

This section provides a functional description of the ADC8 board. See Figure 3 for a block diagram of the ADC8.

The ADC8 is an 8 channel differential input Analog to Digital Converter board. The primary components in each channel are an Input Range Multiplexer, an ADC4322 analog to digital converter, and two 8 bit registers with output enables. An Altera MAX7128 CPLD, called the Clock Control Bus CPLD, provides control for all channels and interfaces with the Clock Control Bus.

The ADC8 boards receive preamplified analog array output signals from the POST[8:1] inputs on the P2 connector. These analog array signals pass through an Input Range Mux and on to the ADCs. The Input Range Mux configures the ADC4322 ADCs input voltage range settings. The ADC4322 ADCs convert the analog signals to digital format. This digital data is clocked into the output registers. The Clock Control Bus CPLD monitors the Clock Control Bus for sequencing which channel's data is output enabled onto the Read Data Bus. The Read Data Bus is the digital output bus from the ADC8 on the P1 connector.

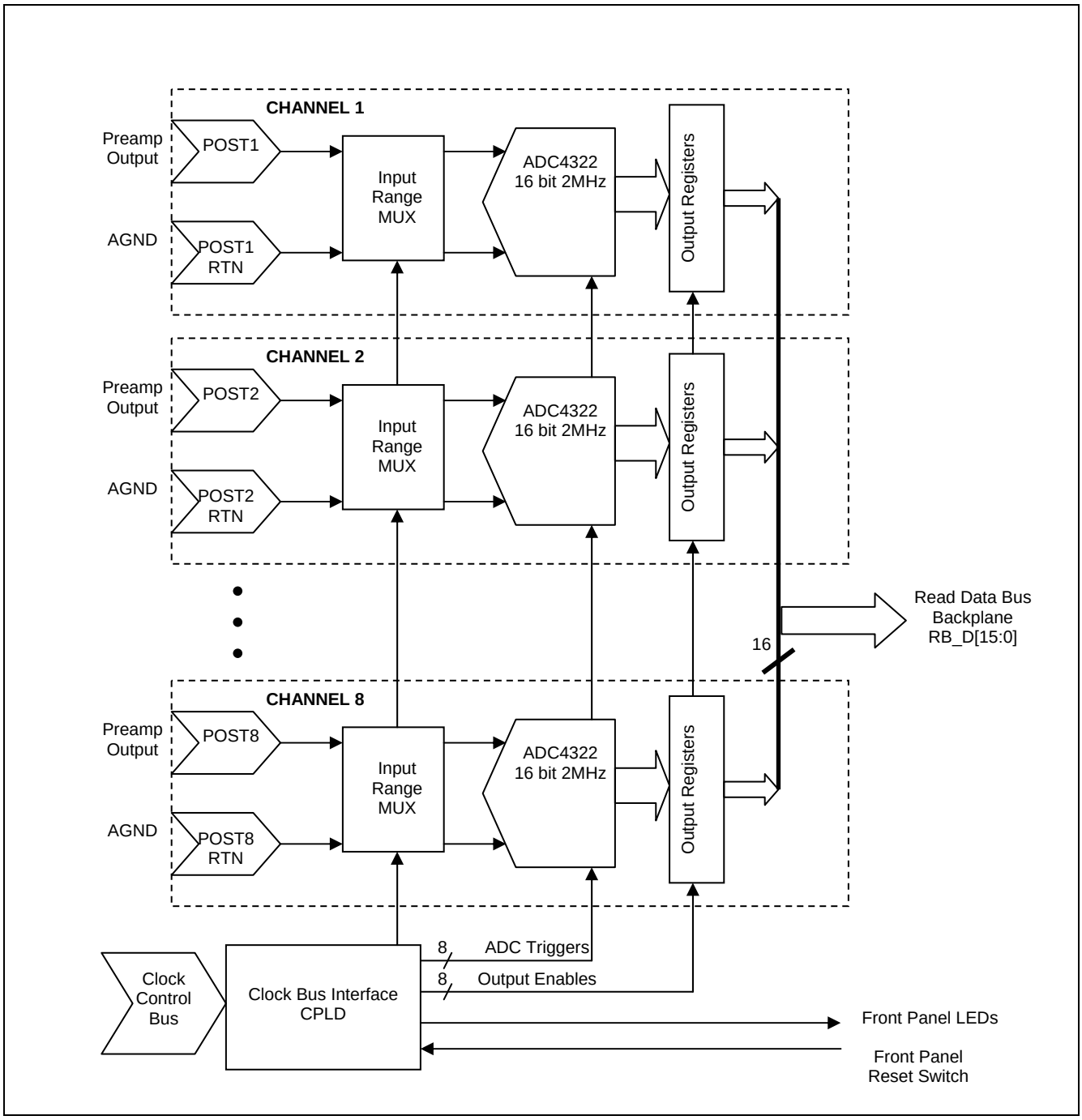

Figure 3 Block Diagram of ADC8

3.1 Inputs

The outputs of a preamplifier board are input (via a backplane ribbon cable) into the ADC8 via the P2 connector. The schematic signal names are 'POST#' (# =1-8) and the other return or reference signals are 'POST# RTN'.

3.2 Input Range Setting, Input Range Mux

An input range select analog multiplexer is configured by U17 an Altera MAX7128 CPLD for a +/- 2.5V range. Alternate settings on the Configuration Header can set the input range for +/-5V or 0-10V range.

3.3 Input Header

An Input Header either selects the normal signal path or analog ground AGND. The normal signal input configuration is pins 1 and 2 shunted.

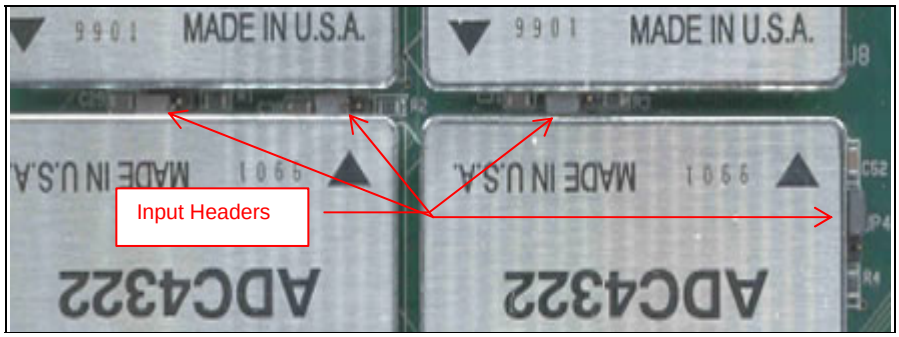

Figure 4 Photo: ADC8 Input Headers

3.4 Analog to Digital Converter

Each of the ADC4322 analog to digital converters is triggered to convert by the TRIG# (#=1-8) signals from U17 MAX7128. The TRIG# signals are derived from the Clock Bus signal CB_D5 (CONVERT). 500 nsec after the rising edge of the TRIG# signal the ADC will complete its conversion and generate a pulse on its TRANSFER output. The rising edge of TRANSFER=XFER# (#=1-8) clocks the 16 bits of digital data present at the ADC outputs into the output registers (74ACT574s).

3.5 Output Sequencing

Each bank of output registers is sequentially enabled (OE#, #=1-8) out to the Read Data Bus based on a state machine design in U17. The Clock Bus signals, CONVERT (CB_D5) initializes the state machine and READ_DATA (CB_D4) enables a counter that sequentially generates the OE# signals on CB_WR! clock signal rising edges.

3.6 Board Configuration, Test Headers

This section describes the ADC8's configuration and test headers. See Figure 5 for a photo of the headers.

JH1 LED/Test Header
JH1 is a 20 pin header that serves the dual purpose of connecting the test signals to the front panel LEDs. The four shunts connect the following signals from the CPLD U17 (Altera MAX7128) to the front panel LEDs:
Signal = front panel label
DIAG0 = ADDR0
DIAG1 = ADDR1
DIAG2 = OE
DIAG3 = CONVERT

JH2 CPLD Configuration Header
JH2 provides input configuration control for the CPLD U5. The default configuration is the only implemented mode.

JTAG Header
The JTAG header is used to program the MAX7128 CPLD.

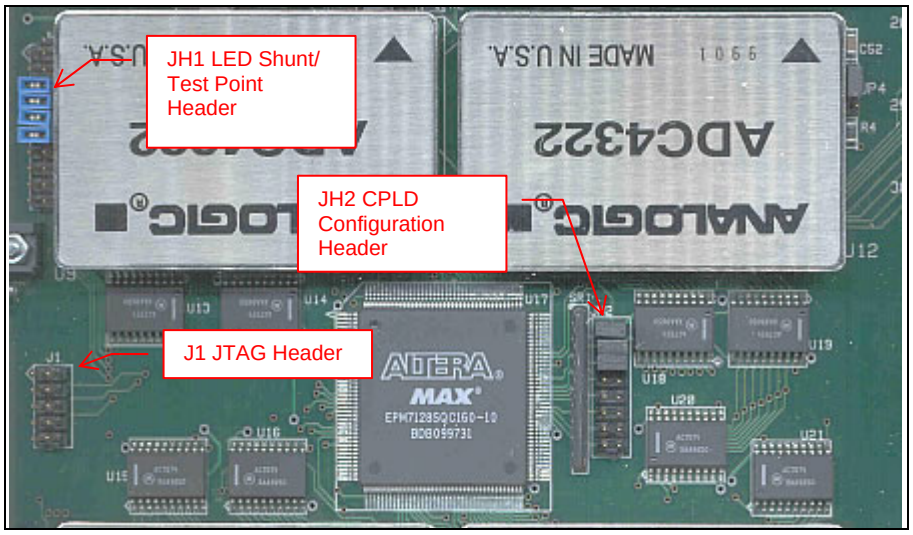

Figure 5 Photo: ADC8 Configuration and Test Headers

4 I/O

This section defines the Inputs and Outputs of the ADC8. All of the ADC8's I/O are via 2 backplane connectors. Each connector has 3 columns of 32 pins. The left column of pins is column C, the middle B, the right A. The top connector is referred to as P1 and the bottom is referred to as P2. The P1 portion of the backplane is implemented as the P2 connections are defined in the VME standard, not as P1 is defined in the VME standard. Both the P1 and P2 connectors have shared B column pins that connect to a bus with standard termination. The A and C column pins are custom defined.

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4.1 P1 Connector Pinout

The signals RB_RD!, RB_D[15:0], and RB_SD[7:0] make up the Read Data Bus.

The "I/O/Bi" column indicates whether the signal is an Input (I), Output (O), or Bidirectional (Bi). This column also indicates whether the signal is a Digital (D), Analog (A), or a Power (PWR) signal.

Col. C Pins	Signal	I/O/Bi	Col. B Pins	Signal	I/O/Bi	Col. A Pins	Signal	I/O/Bi
P1 C1	*Unused*	-	P1 B1	+5V	PWR	P1 A1	+15V	PWR
P1 C2	*Unused*	-	P1 B2	DGND	PWR	P1 A2	AGND	PWR
P1 C3	*Unused*	-	P1 B3	RB_RD!	D I O	P1 A3	*Unused*	-
P1 C4	*Unused*	-	P1 B4	RB_D0	D O	P1 A4	*Unused*	-
P1 C5	*Unused*	-	P1 B5	RB_D1	D O	P1 A5	*Unused*	-
P1 C6	*Unused*	-	P1 B6	RB_D2	D O	P1 A6	*Unused*	-
P1 C7	*Unused*	-	P1 B7	RB_D3	D O	P1 A7	*Unused*	-
P1 C8	*Unused*	-	P1 B8	RB_D4	D O	P1 A8	*Unused*	-
P1 C9	*Unused*	-	P1 B9	RB_D5	D O	P1 A9	*Unused*	-
P1 C10	*Unused*	-	P1 B10	RB_D6	D O	P1 A10	*Unused*	-
P1 C11	*Unused*	-	P1 B11	RB_D7	D O	P1 A11	*Unused*	-
P1 C12	*Unused*	-	P1 B12	DGND	PWR	P1 A12	AGND	PWR
P1 C13	*Unused*	-	P1 B13	+5V	PWR	P1 A13	*Unused*	-
P1 C14	*Unused*	-	P1 B14	RB_D8	D O	P1 A14	*Unused*	-
P1 C15	*Unused*	-	P1 B15	RB_D9	D O	P1 A15	*Unused*	-
P1 C16	*Unused*	-	P1 B16	RB_D10	D O	P1 A16	*Unused*	-
P1 C17	*Unused*	-	P1 B17	RB_D11	D O	P1 A17	*Unused*	-
P1 C18	*Unused*	-	P1 B18	RB_D12	D O	P1 A18	*Unused*	-
P1 C19	*Unused*	-	P1 B19	RB_D13	D O	P1 A19	*Unused*	-
P1 C20	*Unused*	-	P1 B20	RB_D14	D O	P1 A20	*Unused*	-
P1 C21	*Unused*	-	P1 B21	RB_D15	D O	P1 A21	*Unused*	-
P1 C22	*Unused*	-	P1 B22	DGND	PWR	P1 A22	AGND	PWR
P1 C23	*Unused*	-	P1 B23	RB_SD0	D O	P1 A23	*Unused*	-
P1 C24	*Unused*	-	P1 B24	RB_SD1	D O	P1 A24	*Unused*	-
P1 C25	*Unused*	-	P1 B25	RB_SD2	D O	P1 A25	*Unused*	-
P1 C26	*Unused*	-	P1 B26	RB_SD3	D O	P1 A26	*Unused*	-
P1 C27	*Unused*	-	P1 B27	RB_SD4	D O	P1 A27	*Unused*	-
P1 C28	*Unused*	-	P1 B28	RB_SD5	D O	P1 A28	*Unused*	-
P1 C29	*Unused*	-	P1 B29	RB_SD6	D O	P1 A29	*Unused*	-
P1 C30	*Unused*	-	P1 B30	RB_SD7	D O	P1 A30	*Unused*	-
P1 C31	*Unused*	-	P1 B31	DGND	PWR	P1 A31	AGND	PWR
P1 C32	*Unused*	-	P1 B32	+5V	PWR	P1 A32	-15V	PWR

4.2 P2 Connector Pinout

The signals CB_WR!, CB_D[15:0], and CB_CW[7:0] make up the Clock Control Bus. The signals POST[8:1] are preamplified analog array readout signals and POST[8:1]RTN are their corresponding ground signals.

The "I/O/Bi" column indicates whether the signal is an Input (I), Output (O), or Bidirectional (Bi). This column also indicates whether the signal is a Digital (D), Analog (A), or a Power (PWR) signal.

Col. C Pins	Signal	I/O/Bi	Col. B Pins	Signal	I/O/Bi	Col. A Pins	Signal	I/O/Bi
P2 C1	*Unused*	-	P2 B1	+5V	PWR	P2 A1	+15V	PWR
P2 C2	AGND	A I	P2 B2	DGND	PWR	P2 A2	AGND	PWR
P2 C3	POST1	A I	P2 B3	CB_WR!	D I	P2 A3	POST1RTN	A I
P2 C4	AGND	A I	P2 B4	CB_D0	D I	P2 A4	AGND	A I
P2 C5	POST2	A I	P2 B5	CB_D1	D I	P2 A5	POST2RTN	A I
P2 C6	AGND	A I	P2 B6	CB_D2	D I	P2 A6	AGND	A I
P2 C7	POST3	A I	P2 B7	CB_D3	D I	P2 A7	POST3RTN	A I
P2 C8	AGND	A I	P2 B8	CB_D4	D I	P2 A8	AGND	A I
P2 C9	POST4	A I	P2 B9	CB_D5	D I	P2 A9	POST4RTN	A I
P2 C10	AGND	A I	P2 B10	CB_D6	D I	P2 A10	AGND	A I
P2 C11	POST5	A I	P2 B11	CB_D7	D I	P2 A11	POST5RTN	A I
P2 C12	AGND	A I	P2 B12	DGND	PWR	P2 A12	AGND	PWR
P2 C13	POST6	A I	P2 B13	+5V	PWR	P2 A13	POST6RTN	A I
P2 C14	AGND	A I	P2 B14	CB_D8	D I	P2 A14	AGND	A I
P2 C15	POST7	A I	P2 B15	CB_D9	D I	P2 A15	POST7RTN	A I
P2 C16	AGND	A I	P2 B16	CB_D10	D I	P2 A16	AGND	A I
P2 C17	POST8	A I	P2 B17	CB_D11	D I	P2 A17	POST8RTN	A I
P2 C18	AGND	A I	P2 B18	CB_D12	D I	P2 A18	AGND	A I
P2 C19	*Unused*	-	P2 B19	CB_D13	D I	P2 A19	*Unused*	-
P2 C20	*Unused*	-	P2 B20	CB_D14	D I	P2 A20	*Unused*	-
P2 C21	*Unused*	-	P2 B21	CB_D15	D I	P2 A21	*Unused*	-
P2 C22	*Unused*	-	P2 B22	DGND	PWR	P2 A22	AGND	PWR
P2 C23	*Unused*	-	P2 B23	CB_CW0	D I	P2 A23	*Unused*	-
P2 C24	*Unused*	-	P2 B24	CB_CW1	D I	P2 A24	*Unused*	-
P2 C25	*Unused*	-	P2 B25	CB_CW2	D I	P2 A25	*Unused*	-
P2 C26	*Unused*	-	P2 B26	CB_CW3	D I	P2 A26	*Unused*	-
P2 C27	*Unused*	-	P2 B27	CB_CW4	D I	P2 A27	*Unused*	-
P2 C28	*Unused*	-	P2 B28	CB_CW5	D I	P2 A28	*Unused*	-
P2 C29	*Unused*	-	P2 B29	CB_CW6	D I	P2 A29	*Unused*	-
P2 C30	*Unused*	-	P2 B30	CB_CW7	D I	P2 A30	*Unused*	-
P2 C31	*Unused*	-	P2 B31	DGND	PWR	P2 A31	AGND	PWR
P2 C32	*Unused*	-	P2 B32	+5V	PWR	P2 A32	-15V	PWR

5 Acronyms and Definitions

ADC	Analog to Digital Converter
AGND	Analog Ground
DGND	Digital Ground
GND	Electrical ground
MKIR	Mauna Kea Infrared