Mauna Kea Infrared
CLKBIAS
8/16 CHANNEL CLOCK/BIAS DRIVER BOARD

MKIR# 700-111-01
Rev 1.7
Last Modified 10/19/2004

Also includes the specification for

CLKDRV 700-155-01
CLKBIAS DAUGHTER DRIVER BOARD

WARNING: **The CLKBIAS board is not compatible with the VME standard**, though it may appear to be. Inserting the CLKBIAS board in a standard VME chassis will likely cause a **catastrophic failure**. Likewise inserting standard VME cards into the chassis is prohibited and extremely risky.

CLKBIAS Rev 1.7

Revision History

Revision	Author	Summary of revisions	Date
1.7	Mike Thompson	Initial release.	10/18/04
1.1	Peter Onaka	Initial Revision	

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1 CLKBIAS Overview

The CLKBIAS board is a component of the Redstar3 array controller. Redstar3 boards are housed in a 63HP chassis called an Array Control Chassis. The function of the CLKBIAS board is to generate analog clock and bias signals for control of an Aladdin Type III 1024x1024 InSb array (Raytheon SB026-S1 Aladdin III 1024 x 1024 InSb Array).

The CLKBIAS board decodes digital Clock Control Bus sequences from the Redstar3's FCRYO2 boards to generate analog clock and control signals for the array. The CLKBIAS boards convert the digital clock signals to analog levels. Some of the analog outputs to the array are constant voltage signals which are driven as "bias" signals from the CLKBIAS board. Other analog outputs to the array are variable signals, or clocks, which are driven as "clock" signals from the CLKBIAS board. These clock and control signals are sent out of the Array Control Chassis over the Array Control cables to the array in the Cryostat.

The CLKBIAS board can be configured to output combinations of analog clock signals and/or analog bias outputs. 16 individual 12 bit digital to analog converters (DACs) act as either bias signals or the high and low rails of an analog clock signal for driving infrared arrays. The DACs are also jumper configurable for either manual DIP switch setting or software programmable. Multilayer printed circuit board construction employs multiple ground/power planes for shielding.

Some photos of the CLKBIAS board are included in this document below. The front panel is pictured in Figure 1. The component side of the CLKBIAS Board, VGGCL Configuration, is pictured in Figure 2. The component side of the CLKBIAS board, VDDCL Configuration, is pictured in Figure 3.

2 Technical Specifications CLKBIAS (700-111-01)

2.1 General Technical Specifications

- 16 individual 12 bit DACs (AD767) with buffered outputs
- Bias 30ppm/C gain drift
- Bias outputs 150mA max output current
- +/- 10 Volt output range
- Analog switch (HI201HS) based clock outputs
- 30nsec typ. 50nsec max switching times
- 6 layer PCB

2.2 Power Requirements

- +5V 209mA Typ.
- +15V 483mA Typ.
- -15V 483mA Typ.

2.3 Mechanical Specifications

- Eurocard 6U (160mm x 233.35mm) Form Factor (***Note****: the card is electrically incompatible with the VME standards*)
- P1 96 pin DIN Connector, P2 DIN 41612, 96 Pin Connector
- 6 Layer PCB Construction with Internal ground and power Layers

Figure 1 Photo: CLKBIAS Board Front Panel

Figure 2 Photo: Component Side of CLKBIAS Board, VGGCL Configuration

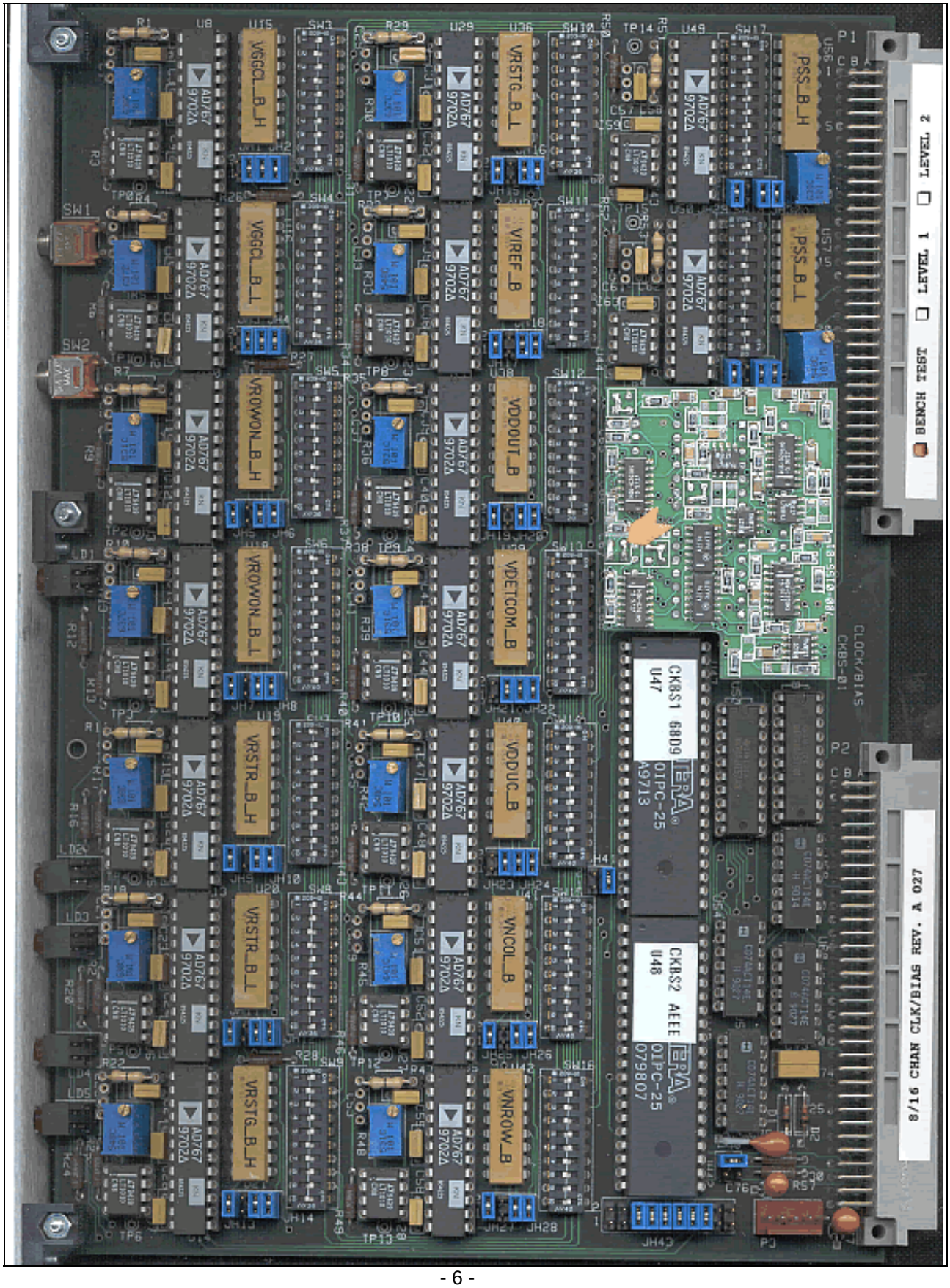
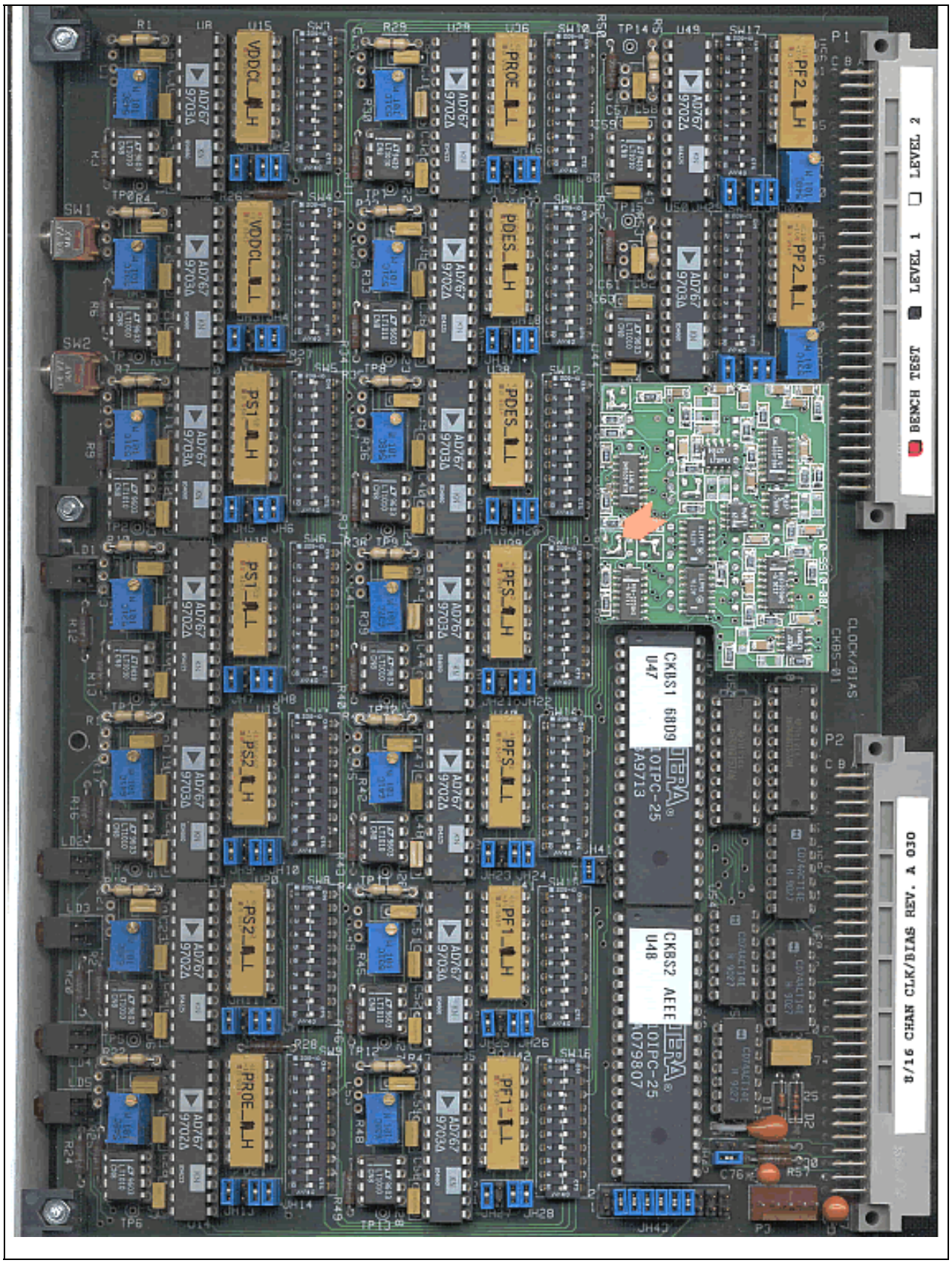


Figure 3 Photo: Component Side of CLKBIAS Board, VDDCL Configuration



3 Functional Description

The Clock Control Bus provides control over the clocks that the CLKBIAS board generates and provides digital clock and bias voltages for programmable DAC circuits. Specific sequences on the Clock Control Bus cause transitions between high and low levels for DACs configured as clocks. The clock and bias signals are output from the CLKBIAS board on the backplane connector.

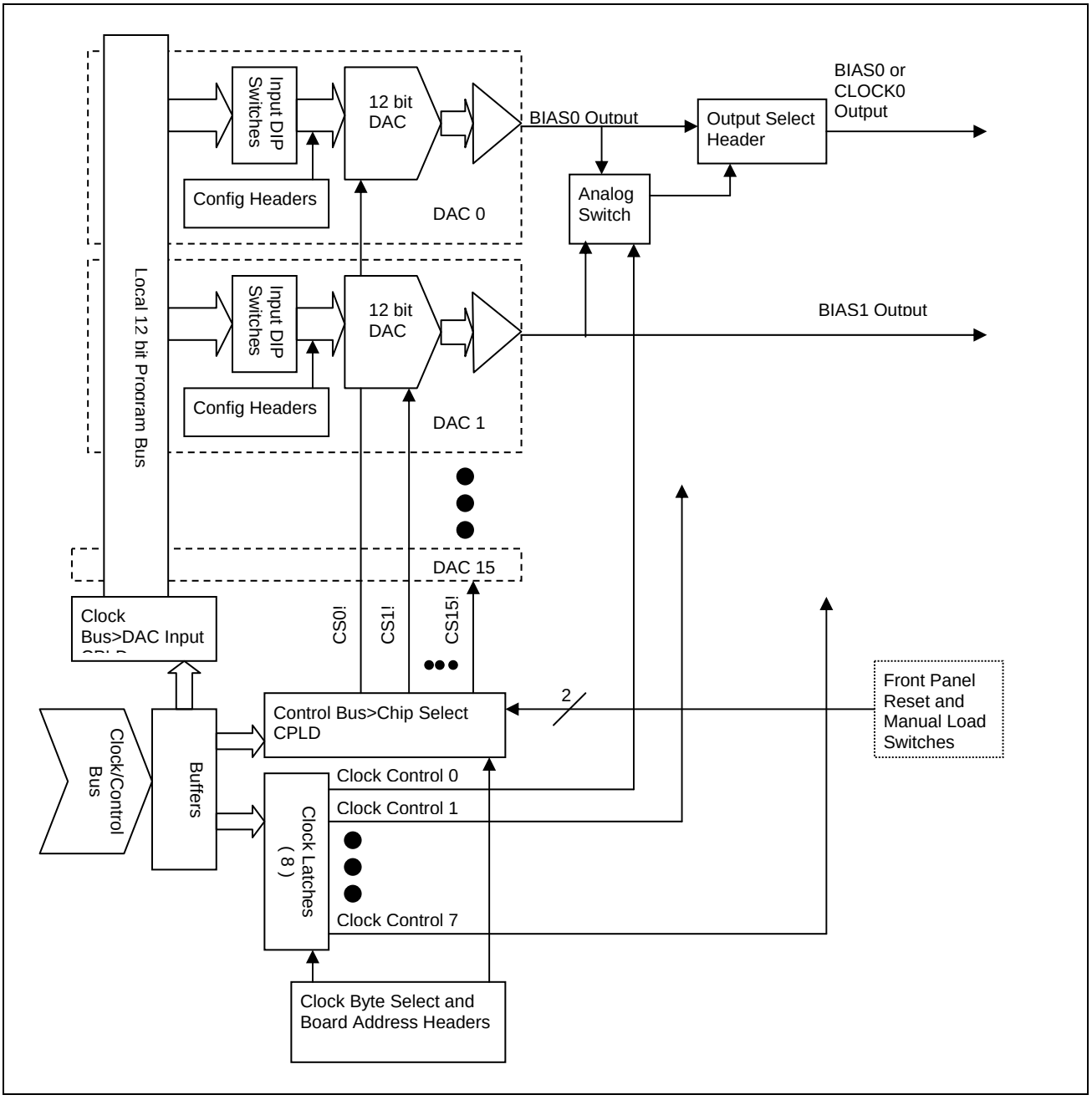


Figure 4 CLKBIAS Block Diagram

3.1 Inputs

The Clock Control Bus signals CB_D0 to CB_D15 are digital bus inputs to the board that are buffered and used to control the analog output switches. In addition the control signals CB_CW0 to CB_CW7 are used to select and program specific DAC circuits that have been shunt enabled to be programmed by the Clock DSP.

3.2 Control CPLDs

Two Altera EP910 CPLDs decode the Control Bus sequences for DAC programming and board control. The Chip Select CPLD, U48 in the schematic, decodes the specific board and DAC address from the Clock Control Bus and generates a Chip Select signal CS0! To CS15!. The DAC Input CPLD, U47 in the schematic, latches the 12 bit DAC program value from a specific Clock Bus cycle.

3.3 Clock and Bias Signal (DAC) Configuration

There are 16 virtually identical DAC circuit sections laid out on the printed circuit board. Each section has a 10 position DIP switch plus 2 headers that connect to the 12 bit input of the DAC. There is also a Manual/Programmable Selection Header. If the header is configured for Manual control (pins 1&2 shunted) then the DAC will output the voltage solely set by the positions on the DIP switch +2 headers. The CPLDs are programmed to output a CS! signal (which loads the 12 bits into the input on CS!'s rising edge) after a power up delay and if the front panel Manual Load switch is pressed. These circuit elements are pictured below in Figure 5.

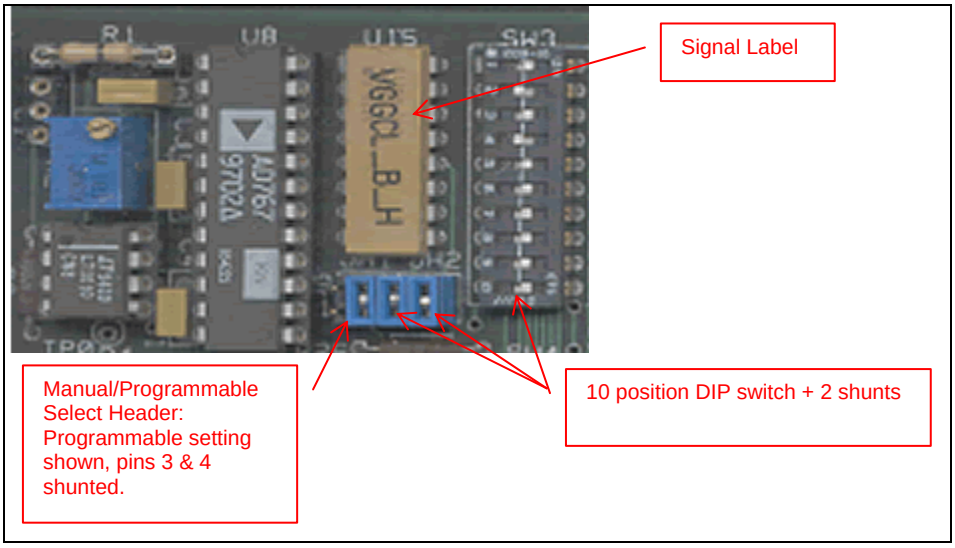


Figure 5 DAC/BIAS Circuit: DIP Switches and Headers

If a particular DAC has been configured to be software programmable, the voltage are can be set by the user in the Engineering Window of the user interface.

3.4 Analog Clock Switches

To create an analog clock signal, two DAC outputs are input into a high speed analog switch (HI201HS). The switch is controlled by the Clock Control 1 – Clock Control 8 signals derived from the Clock Control Bus. For example if the LOW byte is selected, the CB_D0 will control the analog CLK0 switch. A downstream selection header either allows the BIAS or CLK signal to be output by the board.

3.5 Board Configuration, Test Connectors

This section provides details on configuring the CLKBIAS board and explains the functionality of the test headers.

3.5.1 Board Configurations for 1024x1024 InSb arrays (Raytheon 152 and 206 readouts)

The Redstar3 system is configured to run the top 2 quadrants of the array separately from the bottom two. That is to say the top half of the array is run separately from the bottom half. Two CLKBIAS boards are needed to run each half of the array. Consequently there are 4 CLKBIAS boards in the system. They can be

differentiated by the first DAC signal generated by the board and whether they run the top or bottom half of the array. There are 19 identical clock and bias signals for each array half. Thirteen of the array inputs are clock signals. Each clock signal requires 2 of the CLKBIAS' DAC circuits, one for the clock high voltage, and one for the clock low voltage. For each half of the array six of the array inputs are constant voltage, or bias, signals. The bias signals only require one DAC circuit each. Each array half requires 2 CLKBIAS boards for driving all of the control and power signals to the arrays. One of the CLKBIAS boards for each half is implemented in a "VDDCL Configuration" for driving 8 of the clock signals. The other CLKBIAS board is implemented in a "VGGCL Configuration" for driving 5 clock signals and 6 bias signals.

3.5.2 Input Byte Selection, JH41 Header

The Input Byte Selection Header, JH41 on the schematic, selects the upper or lower byte of the Clock Control Bus for use by the CLKBIAS board. Either the lower CB_D0 to CB_D7 or upper CB_D8 to CB_D15 bytes of the Clock Control Bus are selected via JH41. Shunting pins 1 to 2 selects the High Byte. Shunting pins 3 to 4 selects the Low Byte.

See sections 3.5.3 and 3.5.4 for specifics on the input byte selection configuration for this project.

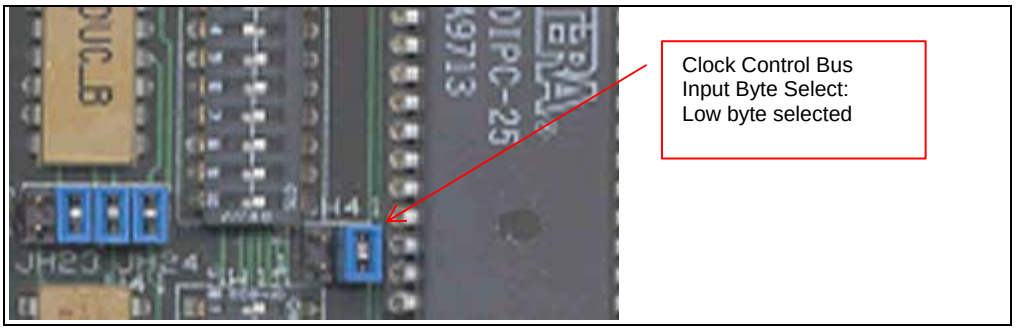


Figure 6 Photo: Clock Control Bus Input Byte Selection

3.5.3 VGGCL Configuration

A photo of the "VGGCL" configuration is shown in Figure 2. Note that the label reads VGGCL_B_H which is the VGGCL signal for the bottom half ('_B') of the array and the pictured DAC circuit supplies the high level ('_H'). The High level corresponds to the digital high state of the corresponding Clock/Control Bus signal. The Input Byte Selection Header is set for the LOW byte so the analog clock signal VGGCL is controlled by CB_D0. A similarly configured board is used for the top 2 halves of the array.

3.5.4 VDDCL Configuration

A photo of the "VDDCL" configuration is shown in Figure 3. Note that the label reads VDDCL_x_H which is the VDDCL signal for the spare (x) board of the array and the DAC circuit supplies the High level. The High level ('_H') corresponds to the digital high state of the corresponding Clock/Control Bus signal. The Input Byte Selection Header is set for the HIGH byte so the analog clock signal VDDCL is controlled by CB_D8.

3.5.5 Standard voltage settings

The Bias and Clock voltage settings for the 1024 x 1024 InSb Raytheon 152 and 206 readouts are shown in Figure 7. Note that the voltages that are set to programmable ranges will be initialized by the CPLDs and DIP switches to the most negative value in the range, i.e. VDETCOM, VDDUC and VGGCL will be initialized to –3.75 volts. The system is shipped configured such that only the VGGCL (DAC0), VDETCOM (DAC10), and VDDUC (DAC11) voltages are programmable. **It is absolutely critical that VDETCOM be set to a more positive voltage than VDDUC or the array can be critically damaged**

These voltage settings have been optimized through extensive testing. The arrays are very sensitive devices. Extreme care must be exercised if these voltages are to be changed.

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BIAS VOLTAGES AS OF 3/20/98 USING some FOWLER VOLTAGES

DETECTOR BIAS			1 LSB = VOLTS	DIP SWITCH POSITION 1	2	3	4	5	6	7	8	9	10	JHX	JHXX
VDDUC	***VDETCOM***		9.995117188	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
-3.7	-3.375														
		signal													
Board #	DAC#	***Italics = set for programmable voltage, voltage shown is max negative***													
			0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	0	VDDCL_B_H	-4.5	ON	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON
0	1	VDDCL_B_L	-1.3	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF
0	2	PS1_B_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	3	PS1_B_L	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
0	4	PS2_B_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	5	PS2_B_L	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
0	6	PROE_B_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	7	PROE_B_L	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
0	8	PDES_B_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	9	PDES_B_L	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
0	10	PFS_B_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	11	PFS_B_L	-4	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON
0	12	PF1_B_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	13	PF1_B_L	-4	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON
0	14	PF2_B_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	15	PF2_B_L	-4	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON
1	0	***VGGCL_B_H****	***-3.75***	ON	OFF	ON	OFF	ON	ON	ON	ON	ON	ON	ON	ON
1	1	VGGCL_B_L	-4.5	ON	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON
1	2	VROWON_B_H	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
1	3	VROWON_B_L	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
1	4	VRSTR_B_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
1	5	VRSTR_B_L	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
1	6	VRSTG_B_H	-2	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON
1	7	VRSTG_B_L	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
1	8	VIREF_B	-1.8	ON	OFF	OFF	ON	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
1	9	VDDOUT_B	-1.3	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF
1	10	***VDETCOM_B****	***-3.75***	ON	OFF	ON	OFF	ON	ON	ON	ON	ON	ON	ON	ON
1	11	***VDDUC_B****	***-3.75***	ON	OFF	ON	OFF	ON	ON	ON	ON	ON	ON	ON	ON
1	12	VNCOL_B	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
1	13	VNROW_B	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
1	14	PSS_B_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
1	15	PSS_B_L	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF

Figure 7 Table of Standard BIAS and Clock Voltage Settings

3.5.6 JH43 Front Panel LED/Test Header

JH43 is a 20 pin header that serves the dual purpose of connecting the test signals to the front panel LEDs. The five shunts connect the following signals from the CPLD U48 to the front panel LEDs:

Signal = front panel label
STAT0 = !RST board reset indicator
STAT1 = ADDR0 board address0
STAT2 = ADDR1 board address1
STAT3 = HI/LO high/low byte select
STAT4 = THISBD board being addressed by control sequence

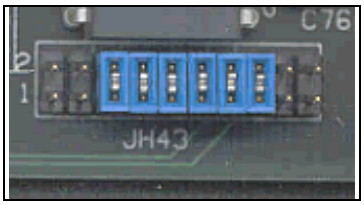

Figure 8 Photo: JH43 LED/Test Header

When used as a test header, the signals are configured to mate with an HP 1600 series Logic Analyzer 16 channel pod.

3.5.7 JH42 CPLD Board Address Header

JH42 sets the board address for each half of the array electronics. The VGGCL boards are set with pins 3 and 4 shunted which sets ADDR1=0, ADDR0=1 board address=1.

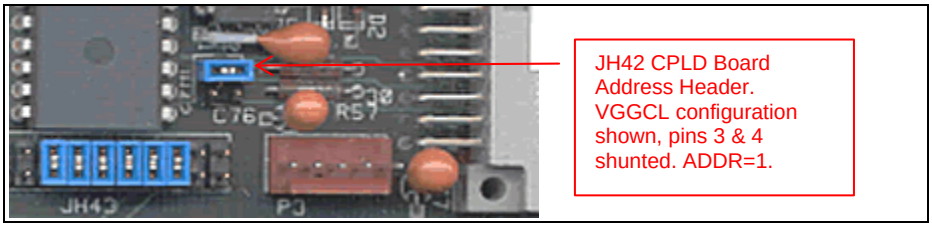

Figure 9 Photo: JH42 CPLD Board Address Header, VGGCL Configuration

The VDDCL boards are set with pins 1 and 2 shunted which sets ADDR1=1, ADDR0=0 board address=2.

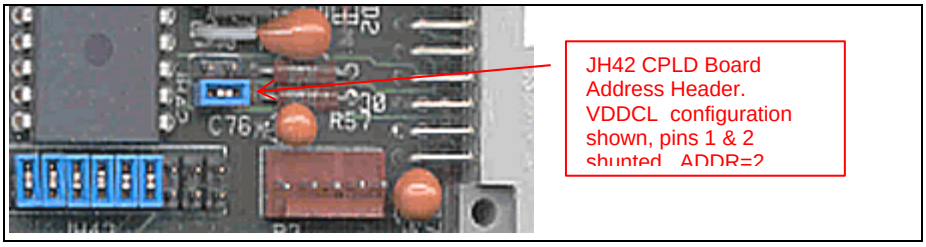

Figure 10 Photo: JH42 CPLD Board Address Header, VDDCL Configuration

3.5.8 Manual Load and Reset Front Panel Switches

Neither of the front panel switches are needed for normal system operation. They are useful for checkout and troubleshooting. When either switch is depressed, the DACs will be programmed with whatever is set on the DIP switches and will override any previous programmed voltage. Manual load is a bit more useful for bench top testing.

3.6 700-155-01 CLKBIAS Daughter Driver Board

3.6.1 Overview

Each VGGCL and VDDCL configured CLKBIAS board has an associated 700-154-01 daughter board that provides high speed analog clocking on each of the 8 output clocks. In addition, the first 4 clocks can be jumper solder configured for output through a 2 pole Bessel filter for delayed rise and fall times.

3.6.2 Technical Specifications

- HS201HS analog switches, clocks channels 1-8
- Harris 5127 opamp based Bessel filter on clocks channels 1-4
- Surface mount daughter board for 700-0111-1 CLKBIAS boards

3.6.3 Component side photographs of configured daughter boards

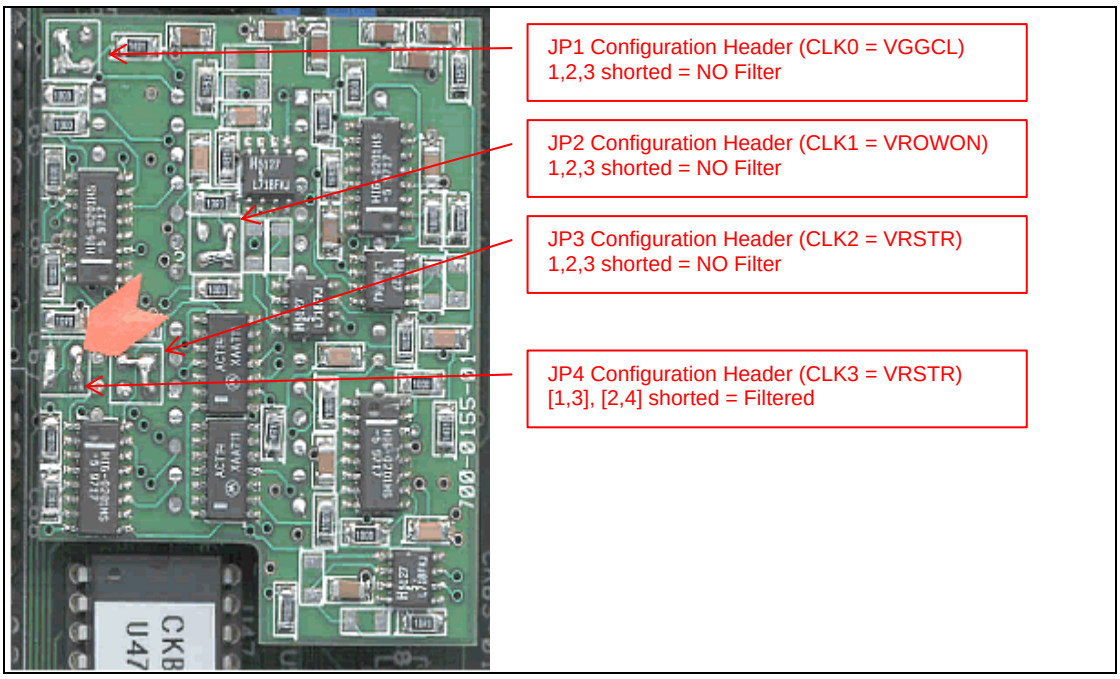

Figure 11 Photo: CLKBIAS Daughter Board, VGGCL configuration

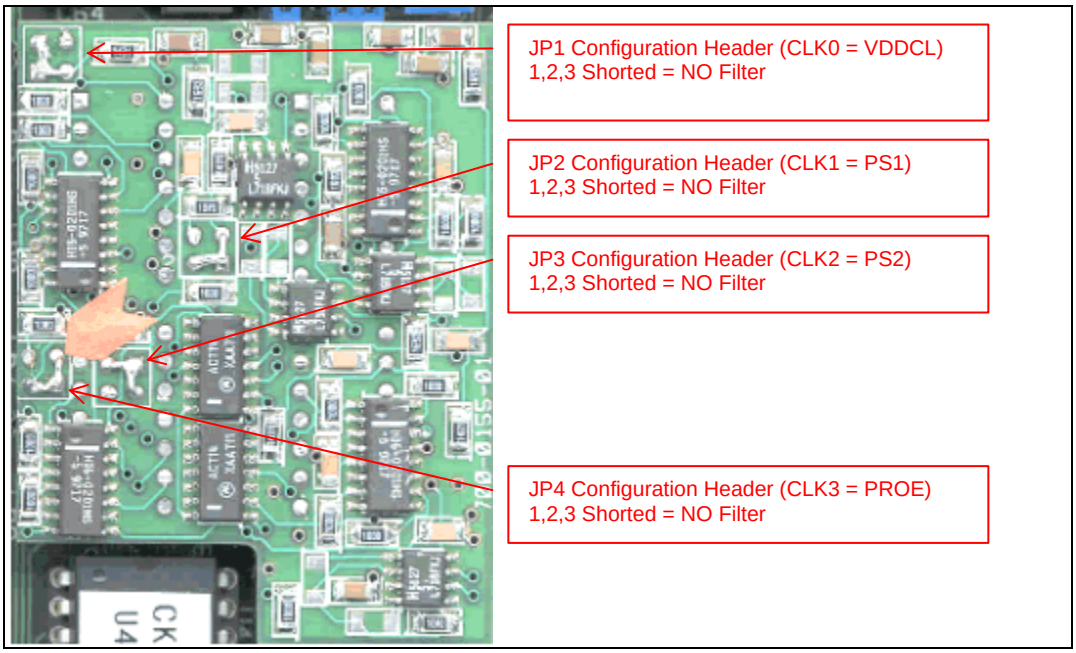

Figure 12 Photo: CLKBIAS Daughter Board, VDDCL configuration

4 I/O

This section defines the Inputs and Outputs of the CLKBIAS board. All of the CLKBIAS' I/O are via 2 backplane connectors. Each connector has 3 columns of 32 pins. The top connector is referred to as P1 and the bottom is referred to as P2. The pin configuration is for the Backplane is based on the VME P2 backplane standard electrically, but do perform the same functions (the board is not VME compliant). Both the P1 and P2 connectors have shared B column pins that connect to a bus with standard terminations. The A and C column pins are custom defined.

WARNING: **The CLKBIAS board is not compatible with the VME standard**, though it may appear to be. Inserting the CLKBIAS board in a standard VME chassis will likely cause a **catastrophic failure**. Likewise inserting standard VME cards into the chassis is prohibited and extremely risky.

Clock and BIAS Outputs: The 16 outputs of the CLKBIAS board are output on the P1 connector.

Clock Control Bus: The Clock Control Bus is a digital input to the CLKBIAS board from the backplane P2 connector. There are 3 parts of the bus. The CB_D[15:0] signals control the analog output switches. The bus also contains control signals CB_CW[7:0] which are used to select and program specific DAC circuits that have been shunt enabled to be programmed by the Clock DSP. CB_WR! controls latching of the Clock Control Bus by the CLKBIAS board.

4.1 P1 Connector Pinout

The “I/O/Bi” column indicates whether the signal is an Input (I), Output (O), or Bidirectional (Bi). This column also indicates whether the signal is a Digital (D), Analog (A), or a Power (PWR) signal.

Col. C Pins	Signal	I/O/Bi	Col. B Pins	Signal	I/O/Bi	Col. A Pins	Signal	I/O/Bi
P1 C1	*Unused*	-	P1 B1	+5V	PWR	P1 A1	+15V	PWR
P1 C2	*Unused*	-	P1 B2	DGND	PWR	P1 A2	AGND	PWR
P1 C3	*Unused*	-	P1 B3	RB_RD!	D I	P1 A3	*Unused*	-
P1 C4	*Unused*	-	P1 B4	RB_D0	D I	P1 A4	*Unused*	-
P1 C5	*Unused*	-	P1 B5	RB_D1	D I	P1 A5	*Unused*	-
P1 C6	*Unused*	-	P1 B6	RB_D2	D I	P1 A6	*Unused*	-
P1 C7	*Unused*	-	P1 B7	RB_D3	D I	P1 A7	*Unused*	-
P1 C8	*Unused*	-	P1 B8	RB_D4	D I	P1 A8	*Unused*	-
P1 C9	*Unused*	-	P1 B9	RB_D5	D I	P1 A9	*Unused*	-
P1 C10	*Unused*	-	P1 B10	RB_D6	D I	P1 A10	*Unused*	-
P1 C11	*Unused*	-	P1 B11	RB_D7	D I	P1 A11	*Unused*	-
P1 C12	*Unused*	-	P1 B12	DGND	PWR	P1 A12	AGND	PWR
P1 C13	*Unused*	-	P1 B13	+5V	PWR	P1 A13	*Unused*	-
P1 C14	*Unused*	-	P1 B14	RB_D8	D I	P1 A14	*Unused*	-
P1 C15	*Unused*	-	P1 B15	RB_D9	D I	P1 A15	*Unused*	-
P1 C16	*Unused*	-	P1 B16	RB_D10	D I	P1 A16	*Unused*	-
P1 C17	CK0BS0	A O	P1 B17	RB_D11	D I	P1 A17	AGND	PWR
P1 C18	BIAS1	A O	P1 B18	RB_D12	D I	P1 A18	AGND	PWR
P1 C19	CK1BS2	A O	P1 B19	RB_D13	D I	P1 A19	AGND	PWR
P1 C20	BIAS3	A O	P1 B20	RB_D14	D I	P1 A20	AGND	PWR
P1 C21	CK2BS4	A O	P1 B21	RB_D15	D I	P1 A21	AGND	PWR
P1 C22	BIAS5	A O	P1 B22	DGND	PWR	P1 A22	AGND	PWR
P1 C23	CK3BS6	A O	P1 B23	RB_SD0	D I	P1 A23	AGND	PWR
P1 C24	BIAS7	A O	P1 B24	RB_SD1	D I	P1 A24	AGND	PWR
P1 C25	CK4BS8	A O	P1 B25	RB_SD2	D I	P1 A25	AGND	PWR
P1 C26	BIAS9	A O	P1 B26	RB_SD3	D I	P1 A26	AGND	PWR
P1 C27	CK5BS10	A O	P1 B27	RB_SD4	D I	P1 A27	AGND	PWR
P1 C28	BIAS11	A O	P1 B28	RB_SD5	D I	P1 A28	AGND	PWR
P1 C29	CK6BS12	A O	P1 B29	RB_SD6	D I	P1 A29	AGND	PWR
P1 C30	BIAS13	A O	P1 B30	RB_SD7	D I	P1 A30	AGND	PWR
P1 C31	CK7BS14	A O	P1 B31	DGND	PWR	P1 A31	AGND	PWR
P1 C32	BIAS15	A O	P1 B32	+5V	PWR	P1 A32	-15V	PWR

4.2 P2 Connector Pinout

The “I/O/Bi” column indicates whether the signal is an Input (I), Output (O), or Bidirectional (Bi). This column also indicates whether the signal is a Digital (D), Analog (A), or a Power (PWR) signal.

Col. C Pins	Signal	I/O/Bi	Col. B Pins	Signal	I/O/Bi	Col. A Pins	Signal	I/O/Bi
P2 C1	*Unused*	-	P2 B1	+5V	PWR	P2 A1	+15V	PWR
P2 C2	*Unused*	-	P2 B2	DGND	PWR	P2 A2	AGND	PWR
P2 C3	*Unused*	-	P2 B3	CB_WR!	D I	P2 A3	*Unused*	-
P2 C4	*Unused*	-	P2 B4	CB_D0	D I	P2 A4	*Unused*	-
P2 C5	*Unused*	-	P2 B5	CB_D1	D I	P2 A5	*Unused*	-
P2 C6	*Unused*	-	P2 B6	CB_D2	D I	P2 A6	*Unused*	-
P2 C7	*Unused*	-	P2 B7	CB_D3	D I	P2 A7	*Unused*	-
P2 C8	*Unused*	-	P2 B8	CB_D4	D I	P2 A8	*Unused*	-
P2 C9	*Unused*	-	P2 B9	CB_D5	D I	P2 A9	*Unused*	-
P2 C10	*Unused*	-	P2 B10	CB_D6	D I	P2 A10	*Unused*	-
P2 C11	*Unused*	-	P2 B11	CB_D7	D I	P2 A11	*Unused*	-
P2 C12	*Unused*	-	P2 B12	DGND	PWR	P2 A12	AGND	PWR
P2 C13	*Unused*	-	P2 B13	+5V	PWR	P2 A13	*Unused*	-
P2 C14	*Unused*	-	P2 B14	CB_D8	D I	P2 A14	*Unused*	-
P2 C15	*Unused*	-	P2 B15	CB_D9	D I	P2 A15	*Unused*	-
P2 C16	*Unused*	-	P2 B16	CB_D10	D I	P2 A16	*Unused*	-
P2 C17	*Unused*	-	P2 B17	CB_D11	D I	P2 A17	*Unused*	-
P2 C18	*Unused*	-	P2 B18	CB_D12	D I	P2 A18	*Unused*	-
P2 C19	*Unused*	-	P2 B19	CB_D13	D I	P2 A19	*Unused*	-
P2 C20	*Unused*	-	P2 B20	CB_D14	D I	P2 A20	*Unused*	-
P2 C21	*Unused*	-	P2 B21	CB_D15	D I	P2 A21	*Unused*	-
P2 C22	*Unused*	-	P2 B22	DGND	PWR	P2 A22	AGND	PWR
P2 C23	*Unused*	-	P2 B23	CB_CW0	D I	P2 A23	*Unused*	-
P2 C24	*Unused*	-	P2 B24	CB_CW1	D I	P2 A24	*Unused*	-
P2 C25	*Unused*	-	P2 B25	CB_CW2	D I	P2 A25	*Unused*	-
P2 C26	*Unused*	-	P2 B26	CB_CW3	D I	P2 A26	*Unused*	-
P2 C27	*Unused*	-	P2 B27	CB_CW4	D I	P2 A27	*Unused*	-
P2 C28	*Unused*	-	P2 B28	CB_CW5	D I	P2 A28	*Unused*	-
P2 C29	*Unused*	-	P2 B29	CB_CW6	D I	P2 A29	*Unused*	-
P2 C30	*Unused*	-	P2 B30	CB_CW7	D I	P2 A30	*Unused*	-
P2 C31	*Unused*	-	P2 B31	DGND	PWR	P2 A31	AGND	PWR
P2 C32	*Unused*	-	P2 B32	+5V	PWR	P2 A32	-15V	PWR

5 Test Procedures

5.1 Test level description

All boards have undergone 3 levels of testing:

- Bench Level Test: Intended to be a simple board only test which is performed first and uses simple test equipment. Depending on the complexity of the board, the test may only cover a small part of the board functionality.
- Level 1 Test: Should not be performed unless a board has passed the Bench level test. Intended to test functionality and performance without endangering critical components (such as focal plane arrays).
- Level2 Test: full functional and performance test, often only possible in full system with science grade focal plane.

6 Acronyms and Definitions

CPLD	Complex Programmable Logic Device
CS	Chip Select
DAC	Digital to Analog Converter
DSP	Digital Signal Processor