1 Remote MFB Backplane Signal Mapping

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This table is an attempt to trace pc_remote_bus.vhd from the redline directory redline:/scr2/AO/H85_project/Electronics/Hardware/Mutifunction board bus Rob 14/pc_remote_bus.vhd to the HVA Chassis Backplane. I'm using the board schematic and layout, which Peter says is current, from redline:/scr2/AO/H85_project/Electronics/Hardware/MFB_rev1_current 13/MF BD REV 01.ddb*

Under the **Chip Signal column** the first signal is the CPLD's I/O signal name. Subsequent signals trace the signal back to logic under a VHDL architecture construct, usually backplane_io. The Chip Signals, I/O direction, and Pin #s come from pc_remote_bus.pin under the same directory as the .vhd file.

NOTE: The schematic labels for the XCVRs and the Layout labels don't match. They're listed as **Schematic Label/Layout label**. For example in the Pin# 3 row, U43 is the transceiver's label in the schematic and U19 is the transciever's label in the layout.

Some signals pass thruough a transceiver, the input signal to the XCVR is under column **Schematic Signal 1**, the output signal from the XCVR is under column **Schematic Signal 2**. Each XCVR has 2 sets of 8-bit Data I/O, A[8:1] and B[8:1], these are shown along with pin numbers.

Pin#	I/O	Chip Signal	Schematic Signal 1	Schematic Signal 2	J1 Pin
3	O	bpctrl_h_tristate, bp_data_tristate	CTRL_H_ENABLE, U43/U19 XCVR OE!	same	-
4	O	bpd_l_tristate, bp_data_tristate	DATA_L_ENABLE, U40/U16 XCVR OE!	same	
5	O	bpctrl_l_dir <= '0'	CTRL_L_DIR, U44/U20 XCVR Tx_Rx!	same	
6		-	TCLK		
7	O	bpctrl_l_tristate <= '0'	CTRL_L_ENABLE, U44/U20 XCVR OE!	same	
8	O	bpctrl_h_dir <= '0'	CTRL_H_DIR, U43/U19 XCVR Tx_Rx!	same	
9	O	bpd_l_dir <= ! bp_direction_is_write	DATA_L_DIR, U40/U16 XCVR Tx_Rx!	same	
10		GND			
11	I/O	bpctrl(0), bp_direction_is_write, bp_data_direction_is_write	CTRL[0], U44/U20 XCVR B1 pin 18	R_CTRL[0], U44/U20 XCVR A1 pin 2	B3, A1
12	O	bpctrl(1), sinphase_zeros (chip input)	CTRL[1] U44/U20 XCVR B2 pin 17	R_CTRL[1], U44/U20 XCVR A2 pin 3	A2
13	O	bpctrl(2), bp_strobe	CTRL[2] U44/U20 XCVR B3 pin16	R_CTRL[2] U44/U20 XCVR A3 pin4	A3
14	O	bpctrl(3), reset_counters	CTRL[3] U44/U20 XCVR B4 pin 15	R_CTRL[3] U44/U20 XCVR A4 pin5	A4
15	I/O	bpctrl(4), data_from_pc[6], il_io[6]	CTRL[4] U44/U20 XCVR B5 pin 14	R_CTRL[4] U44/U20 XCVR A5 pin6	A5
16	I/O	bpctrl(5), data_from_pc[7], il_io[7]	CTRL[5] U44/U20 XCVR B6 pin 13	R_CTRL[5] U44/U20 XCVR A6 pin7	A6

Pin#	I/O	Chip Signal	Schematic Signal 1	Schematic Signal 2	J1 Pin
17	I/O	bpctrl(6), data_from_pc[8], il_io[8]	CTRL[6] U44/U20 XCVR B7 pin 12	R_CTRL[6] U44/U20 XCVR A7 pin8	A7
18	I/O	bpctrl(7), data_from_pc[9], il_io[9]	CTRL[7] U44/U20 XCVR B8 pin 11	R_CTRL[7] U44/U20 XCVR A8 pin9	A8
23	I/O	bpctrl(8), data_from_pc[10], il_io[10] (duplicates bpctrl(10))	CTRL[8], U43/U19 XCVR B1 pin 18	R_CTRL[8], U43/U19 XCVR A1 pin 2	A10
24	-	UNDEFINED	CTRL[9] U43/U19 XCVR B2 pin 17	R_CTRL[9], U43/U19 XCVR A2 pin 3	A12
25	I/O	bpctrl(10), data_from_pc[10] (duplicates bpctrl(8))	CTRL[10] U43/U19 XCVR B3 pin16	R_CTRL[10] U43/U19 XCVR A3 pin4	A13
26	I/O	bpctrl(11), data_from_pc[11]	CTRL[11] U43/U19 XCVR B4 pin 15	R_CTRL[11] U43/U19 XCVR A4 pin5	A14
27	-	UNDEFINED	CTRL[12] U43/U19 XCVR B5 pin 14	R_CTRL[12] U43/U19 XCVR A5 pin6	A16
28	-	UNDEFINED	CTRL[13] U43/U19 XCVR B6 pin 13	R_CTRL[13] U43/U19 XCVR A6 pin7	A18
29	-	UNDEFINED	CTRL[14] U43/U19 XCVR B7 pin 12	R_CTRL[14] U43/U19 XCVR A7 pin8	A23
30	-	UNDEFINED	CTRL[15] U43/U19 XCVR B8 pin 11	R_CTRL[15] U43/U19 XCVR A8 pin9	A24
31	-	GND			
32	I/O	bpaddr(0)	ADDR[0] U42/U18 XCVR B1 pin 18	R_ADDR[0] U42/U18 XCVR B1 pin 2	B22
33	I/O	bpaddr(1)	ADDR[1] U42/U18 XCVR B2 pin 17	R_ADDR[1] U42/U18 XCVR B2 pin 3	B24
34	I/O	bpaddr(2)	ADDR[2] U42/U18 XCVR B3 pin 16	R_ADDR[2] U42/U18 XCVR B3 pin 4	B25
35	I/O	bpaddr(3)	ADDR[3] U42/U18 XCVR B4 pin 15	R_ADDR[3] U42/U18 XCVR B4 pin 5	B26
36	I/O	bpaddr(4)	ADDR[4] U42/U18 XCVR B5 pin 14	R_ADDR[4] U42/U18 XCVR B5 pin 6	B27
37	I/O	bpaddr(5)	ADDR[5] U42/U18 XCVR B6 pin 13	R_ADDR[5] U42/U18 XCVR B6 pin 7	B28
38	I/O	bpaddr(6)	ADDR[6] U42/U18 XCVR B7 pin 12	R_ADDR[6] U42/U18 XCVR B7 pin 8	B29
39	I/O	bpaddr(7)	ADDR[7] U42/U18 XCVR B8 pin 11	R_ADDR[7] U42/U18 XCVR B8 pin 9	B30
40	-	VCC			
41	-	GND			

Pin#	I/O	Chip Signal	Schematic Signal 1	Schematic Signal 2	J1 Pin
42	O	bpd_h_dir, NOT bp_direction_is_write, bp_data_direction_is_write	DATA_H_DIR U41/U17 XCVR Tx_Rx! pin 1	-	-
43	I/O	bpd_h_tristate, bp_data_tristate	DATA_H_ENABLE U41/U17 XCVR OE! pin 19	-	-
44	O	bpaddr_tristate, bp_addr_tristate	ADDR_ENABLE U42/U18 XCVR OE! pin 19	-	-
45	O	bpaddr_dir <= '0' "permanently set to output"	ADDR_DIR U42/U18 XCVR Tx_Rx! pin 1	-	-
46	-	JTAG TMS	no name, J16 10 pin header pin 2	-	-
47	O	led1			
48	O	led2			
49	O	led3			
159	I/O	bpd[15], data_from_pc[5]	D[15], DB[15] U41/U17 XCVR B1 pin 18	RB_D[15] U41/U17 XCVR A1 pin 2	B19
158	I/O	bpd[14], data_from_pc[4]	D[14], DB[14] U41/U17 XCVR B2 pin 17	RB_D[14] U41/U17 XCVR A2 pin 3	B18
157	I/O	bpd[13], data_from_pc[3]	D[13], DB[13] U41/U17 XCVR B3 pin 16	RB_D[13] U41/U17 XCVR A3 pin 4	B17
156	I/O	bpd[12], data_from_pc[2]	D[12], DB[12] U41/U17 XCVR B4 pin 15	RB_D[12] U41/U17 XCVR A4 pin 5	B16
155	I/O	bpd[11], data_from_pc[1]	D[11], DB[11] U41/U17 XCVR B5 pin 14	RB_D[11] U41/U17 XCVR A5 pin 6	B15
154	I/O	bpd[10], data_from_pc[0]	D[10], DB[10] U41/U17 XCVR B6 pin 13	RB_D[10] U41/U17 XCVR A6 pin 7	B14
153	I	bpd[9] ON READ -> read_from_bp_data	D[9], DB[9] U41/U17 XCVR B7 pin 12	RB_D[9] U41/U17 XCVR A7 pin 8	B13
152	I	bpd[8] ON READ -> read_from_bp_data	D[8], DB[8] U41/U17 XCVR B6 pin 11	RB_D[8] U41/U17 XCVR A6 pin 9	B12
150	I	bpd[7] ON READ -> read_from_bp_data	D[7], DB[7] U40/U16 XCVR B1 pin 18	RB_D[7] U40/U16 XCVR A1 pin 2	B30
149	I/O	bpd[6] ON READ -> read_from_bp_data	D[6], DB[6] U40/U16 XCVR B2 pin 17	RB_D[6] U40/U16 XCVR A2 pin 3	B29
148	I/O	bpd[5] ON READ -> read_from_bp_data	D[5], DB[5] U40/U16 XCVR B3 pin 16	RB_D[5] U40/U16 XCVR A3 pin 4	B28
147	I/O	bpd[4] ON READ -> read_from_bp_data	D[4], DB[4] U40/U16 XCVR B4 pin 15	RB_D[4] U40/U16 XCVR A4 pin 5	B27
146	I/O	bpd[3] ON READ -> read_from_bp_data	D[3], DB[3] U40/U16 XCVR B5 pin 14	RB_D[3] U40/U16 XCVR A5 pin 6	B26

Pin#	I/O	Chip Signal	Schematic Signal 1	Schematic Signal 2	J1 Pin
145	I/O	bpd[2] ON READ -> read_from_bp_data	D[2], DB[2] U40/U16 XCVR B6 pin 13	RB_D[2] U40/U16 XCVR A6 pin 7	B25
144	I	bpd[1] ON READ -> read_from_bp_data	D[1], DB[1] U40/U16 XCVR B7 pin 12	RB_D[1] U40/U16 XCVR A7 pin 8	B24
143	I/O	bpd(0), ON READ -> read_from_bp_data	D[0], DB[0] U40/U16 XCVR B6 pin 11	RB_D[0] U40/U16 XCVR A6 pin 9	B22
			dong		

2 BACKPLANE DATA SIGNALS

The signals on the backplane that actually carry the data on writes and reads aren't all on the backplane signals that are called backplane data, RB_D[15:0]. They're spread across RB_D and R_CTRL. Nor do the bit positions that the data is carried on the backplane have any correspondence to the bit position of the word that the server thinks it's writing. This table is an attempt to map out where the data is actually carried and hopefully to figure out why.

Note that here I've boldly presumed that the internal chip signal data_from_pc[15:0], which comes from il_io[15:0], probably from the fiber interface CPLD, has not been munged by the fiber interface CPLD. That is I've used data_from_pc to determine the BP Data Word.

Also bits [15:13] don't seem to be driven to the backplane on writes.

Data Word[15:0], chip pin, BP pin, pin signal, internal signal

In this table BP Data Word represents the proper order of the bits from MSB to LSB. Chip Pin Signal represents the output signal name from the chip's logic to the chip's pin. BP Pin represents the backplane connector pin that carries the signal. Internal signal represents the internal signal in the logic that the pin signal sources.

Here are the signal assignments in the pc_remote_bus CPLD VHDL code.

```
bpd(15 downto 10) <=  data_from_pc(5 downto 0) when (bp_direction_is_write = '1') else (others =>'Z');

bpctrl(7 downto 4) <=  data_from_pc(9 downto 6) when (bp_direction_is_write ='1') else (others =>'Z');

bpctrl(8)          <=  data_from_pc(10) when (bp_direction_is_write ='1') else 'Z';

bpctrl(11 downto 10) <=  data_from_pc(12 downto 11) when (bp_direction_is_write ='1') else (others=>'Z');
```

BP Data Word[15:0]	Chip Pin	Chip I/O	BP Pin	Chip Pin Signal	Internal Chip Signal
15				undefined	
14				undefined	
13				undefined	
12	26	I/O	A14	bpctrl[11]	data_from_pc[12]
11	25	I/O	A13	bpctrl[10]	data_from_pc[11]
10	23	I/O	A10	bpctrl[8]	data_from_pc[10]
9	18	I/O	A8	bpctrl[7]	data_from_pc[9]
8	17	I/O	A7	bpctrl[6]	data_from_pc[8]
7	16	I/O	A6	bpctrl[5]	data_from_pc[7]
6	15	I/O	A5	bpctrl[4]	data_from_pc[6]

BP Data Word[15:0]	Chip Pin	Chip I/O	BP Pin	Chip Pin Signal	Internal Chip Signal
5	159	I/O	B19	bpd[15]	data_from_pc[5]
4	158	I/O	B18	bpd[14]	data_from_pc[4]
3	157	I/O	B17	bpd[13]	data_from_pc[3]
2	156	I/O	B16	bpd[12]	data_from_pc[2]
1	155	I/O	B15	bpd[11]	data_from_pc[1]
0	154	I/O	B14	bpd[10]	data_from_pc[0]