Counter Board

Hardware Design and Test Document

Rev 1.1

Revision History

Date	Rev	Author	Comment
01/22/03	1.0	Rob Yamashita	Initial Document
02/11/03	1.1	Rob Yamashita	Create PDF and add datasheets

1 24 Channel Counter Board

1.1 Overview

The 24 Channel Counter board is used collect counts from 24 independent APDs. Each channel contains a 15 bit counter that counts pulses coming off of an APD. There are two phases for each counter to allow continuous collection of data. Each channel on the board is individually addressable through accesses from the multifunction boards. Additionally you can access each of the phase of the counters while that phase is not counting. Dip switches set the upper three address bits for the board allowing the address range on the board to go from 0-95.

1.2 Technical Specification

- 12 individual Counter channels, 2 phases per Counter
- 15 Bit counters(32768 counts) for each channel and phase

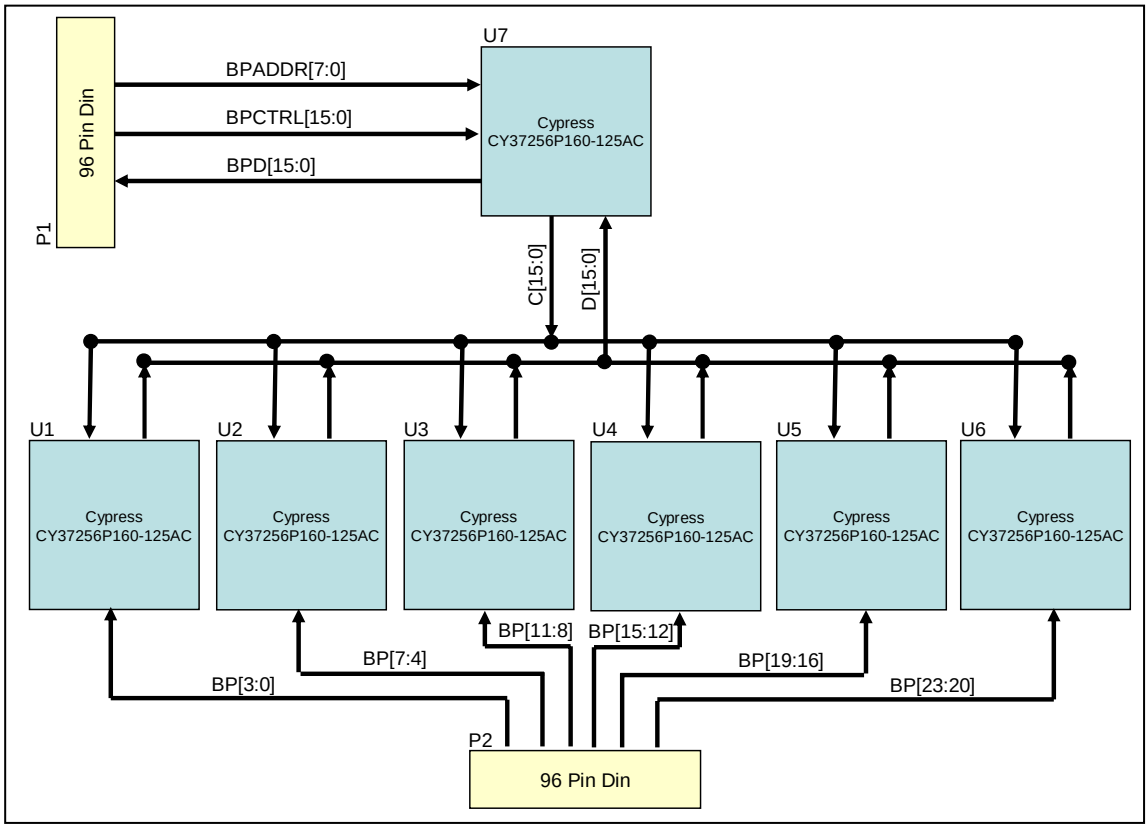
Power Requirements

- +5V
- +12V (Unused on board)
- -12V (Unused on board)

1.3 Mechanical Specification

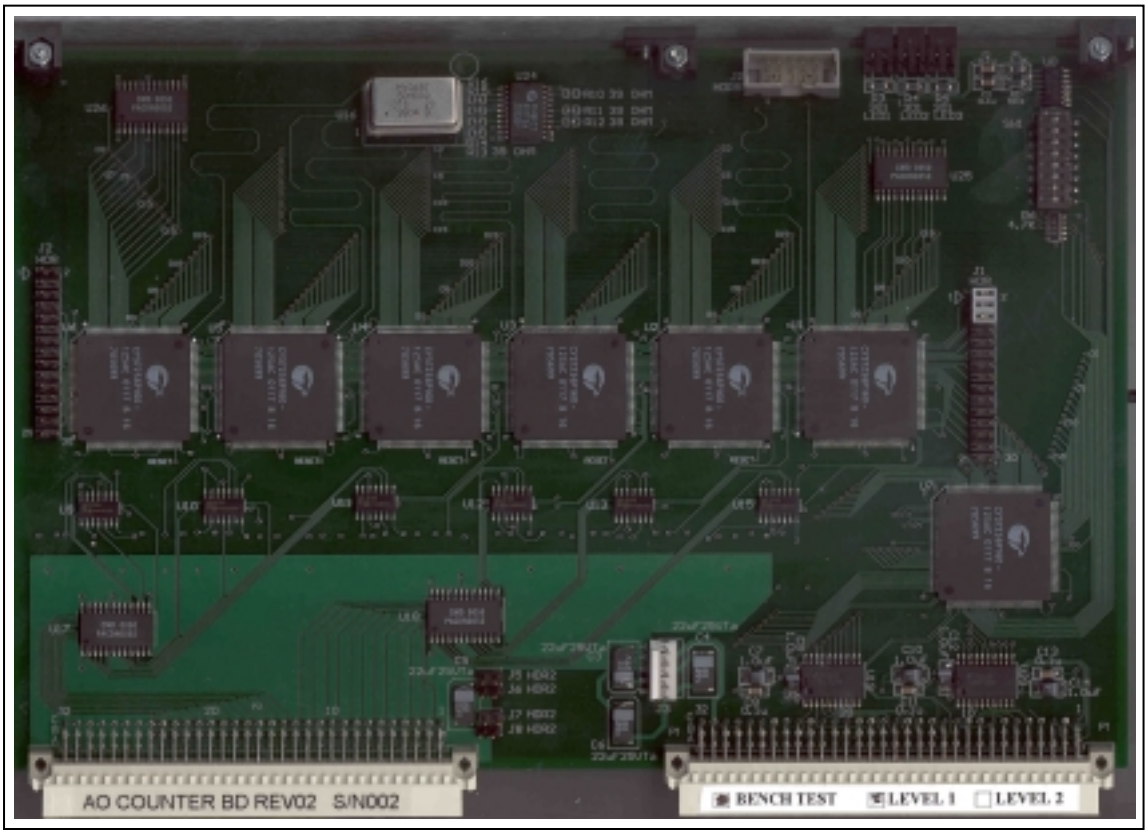
- Eurocard 6U (160mm x 233.35mm) Form Factor
- P1 and P2 96 pin DIN Connector
- 6 Layer PCB Construction

1.4 Block Diagrams

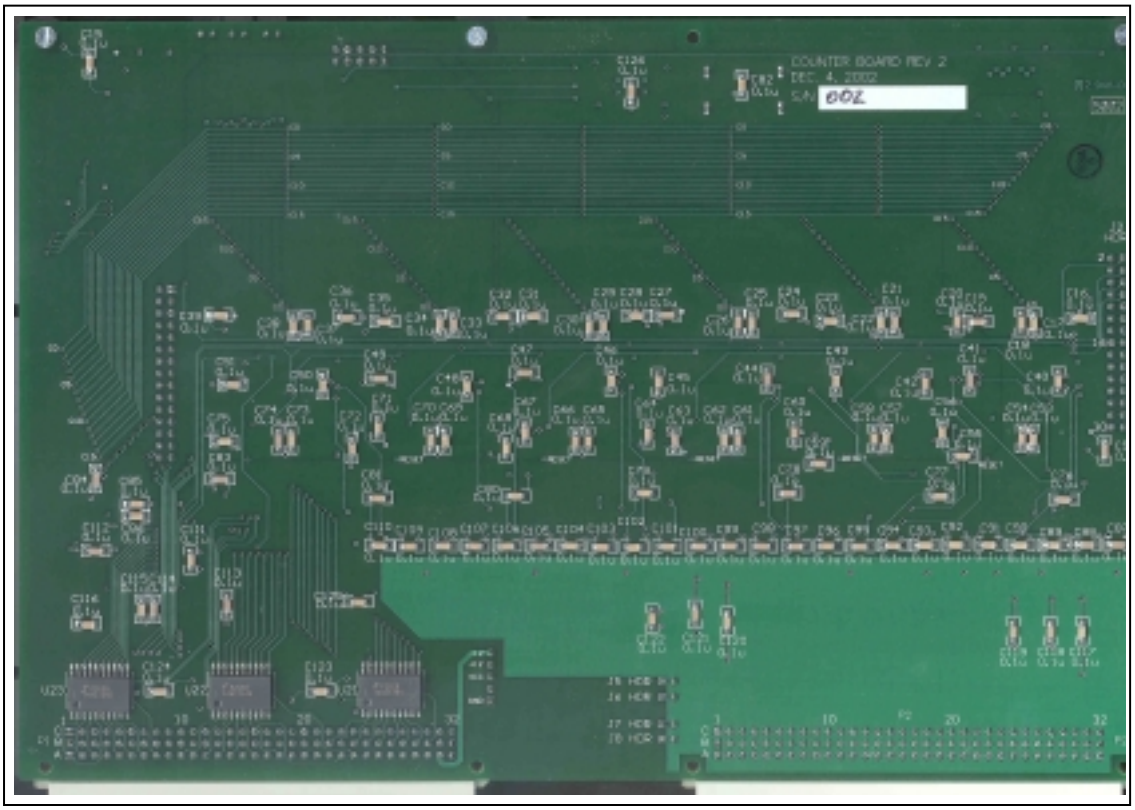


Overall Board Level Block Diagram

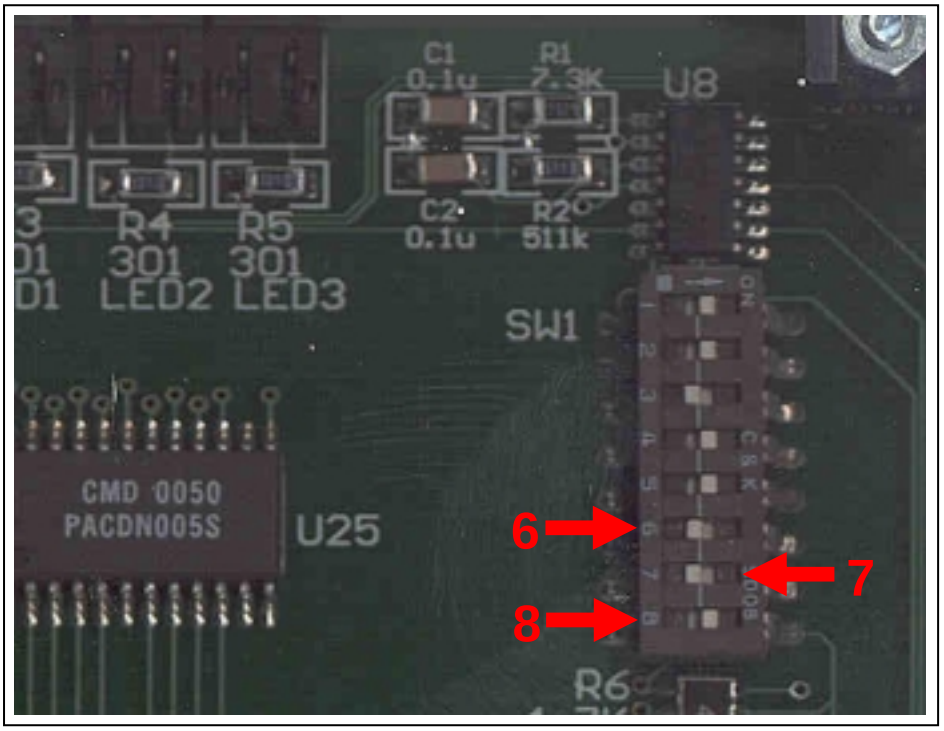
1.5 PCB Layout Front



1.6 PCB Layout Back



1.7 Manual Address Range Select



To set the boards address range switches 6-8 are used.

SW1[8:6]	GUI Address	BPADDR
111	0-23	0-23
110	24-47	32-55
101	48-71	64-87
100	72-95	96-119
Else	nothing	

Note: SW[8:6] correspond to BPADDR[7:5] and set the upper address bits for the boards. BPADDR[4:0] select the channel on the board that is being accessed. BPADDR[4:0] is five bits of address that can address up to 32 different selection, but since there are only 24 channels per board, only 24 of the possible 32 selections access counter channels. All other combinations of BPADDR[4:0] will result in an unknown count. The multifunction board does the translation between the GUI address and the BPADDR and should not put out any of the unknown addresses. A '1' in table corresponds to a 'on' on the switch, a '0' corresponds to 'off'.

2 Test Procedure

2.1 Power Supply Impedance Check

This test is meant to check for shorts between voltage levels and gnd that could cause catastrophic damage to the boards and or power supplies.

Requirements

Digital Multimeter

Procedure

2.4.1. Check GND to VCC by placing one ohm meter lead on GND pin in J3 and other lead on VCC pin in J3

2.4.2. Check GND to +15 by placing one ohm meter lead on GND pin in J3 and other lead on +15 pin in J3

2.4.3. Check GND to -15 by placing one ohm meter lead on GND pin in J3 and other lead on -15 pin in J3

2.4.4. Check VCC to +15 by placing one ohm meter lead on VCC pin in J3 and other lead on +15 pin in J3

2.4.5. Check VCC to +15 by placing one ohm meter lead on VCC pin in J3 and other lead on +15 pin in J3

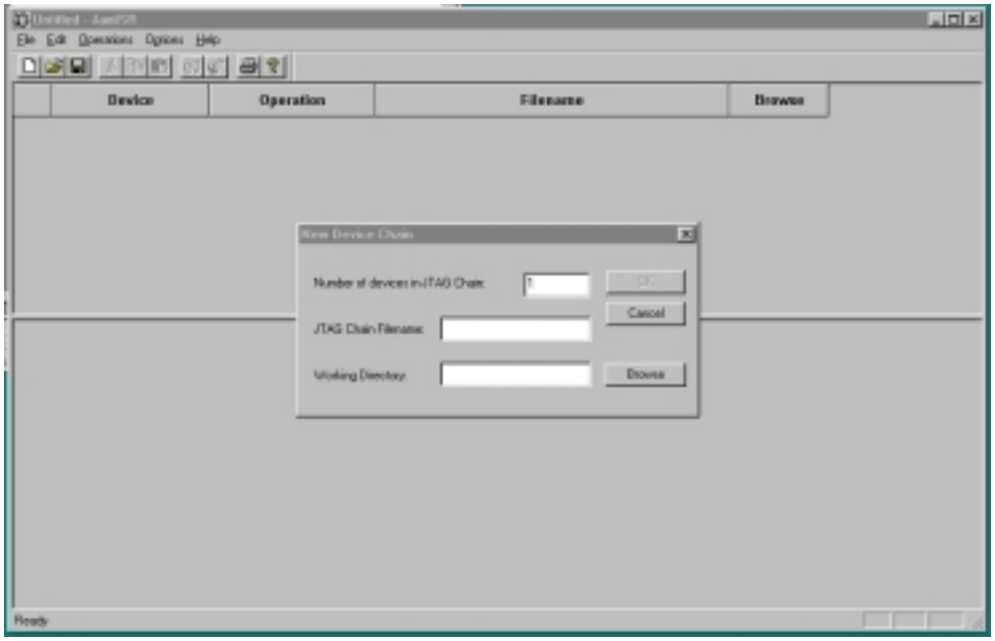
2.4.6. Check +15 to -15 by placing one ohm meter lead on +15 pin in J3 and other lead on -15 pin in J3

2.2 CPLD programming

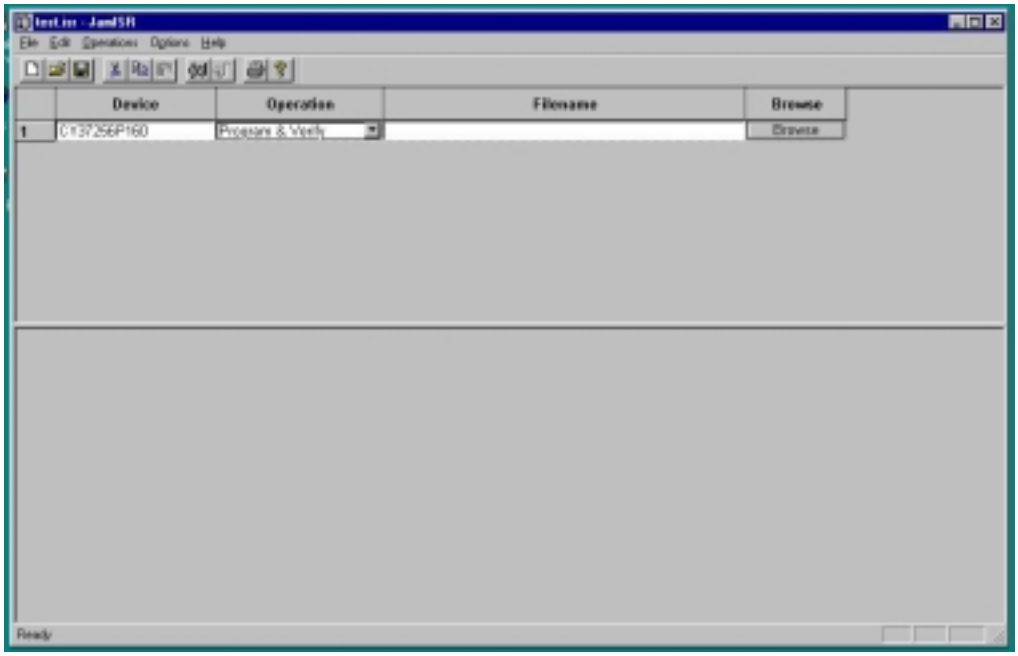
Requirements
Cypress ISR programming software
Cypress UltraISR programming cable
5V power supply
Programming files – "**CounterTop.jed**" dated 1/15/2003 9:05pm
"**Control_Top.jed**" dated 1/02/2003 10:48am

Procedure

2.4.1. Plug Cypress UltraISR programming cable into Parallel port of pc and start Cypress ISR programming software.
2.4.2. Select ‘New’ from the ‘File’ menu



2.4.3. Type ‘7’ in the ‘Number of devices in JTAG Chain’ text box.
2.4.4. Type a filename in the ‘JTAG Chain Filename’ text box.
2.4.5. Browse and select or type in the directory that you would like to save the programming session in.
2.4.6. Press ‘Ok’



2.4.7. In the ‘Devices’ box select ‘CY37256P160’ for all seven of the devices.
2.4.8. In the ‘Operation’ box select ‘Program & Verify’ for all seven of the devices.

2.4.9. Use the ‘Browse’ button for device one to locate and set the path and filename in the ‘filename’ text box to ‘*path*\...\ Control_Top.jed’.

2.4.10. Use the ‘Browse’ button for devices two through seven to locate and set the path and filename in the ‘filename’ text box of each device to ‘*path*\...\ CounterTop.jed’.

2.4.11. Press the  button to compose the programming file.

2.4.12. Plug 5V power and GND into the pins marked “VCC” and “GND” on header J3 respectively.

2.4.13. Connect Cypress UltraISR programming cable to header J16. Connector should be polarized, but if not ensure that pin 1 of cable connects to pin 1 of header.

2.4.14. Turn on power supply.

2.4.15. Press the  button to program the CPLD. Programming may take several minutes to complete

2.4.16. Check log that is displayed to see that each CPLD programmed and verified successfully.

2.4.17. If programming or verify was not successful-

a. Verify that the path and filename are correct in each of the ‘filename’ textboxes. If not, repeat from step 9.

b. Check to see that power and ground are connected correctly and that supply voltage is set to 5V DC. If not, repeat form step 11.

c. Check to see that part is correct and it is soldered correctly to board. If not, correct problem and repeat from step 11.

2.4.18. Turn off power supply and disconnect cables.

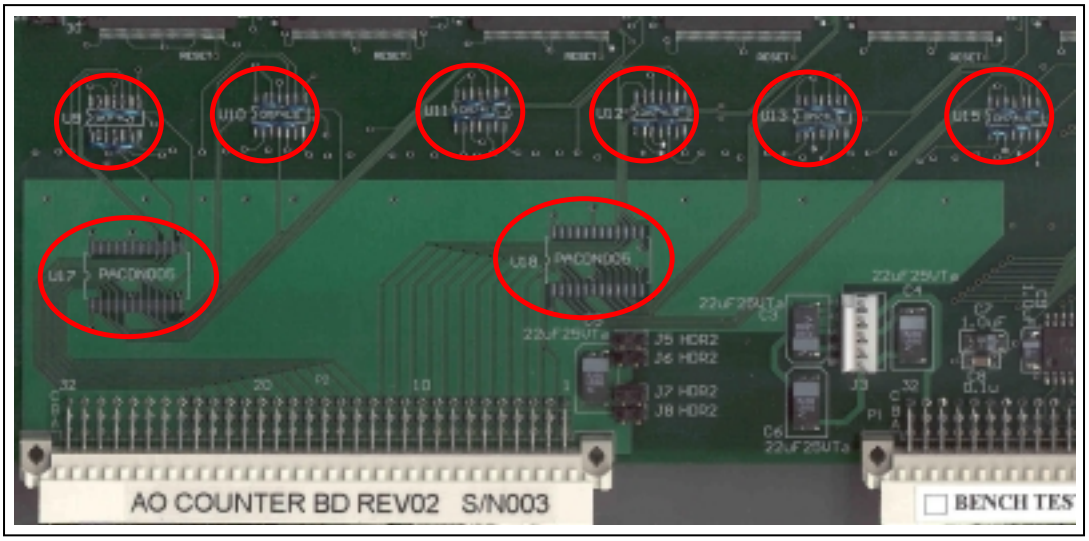
2.3 Test board Rework

2.4.1. Do Not Install Components – U17-U18, U9-U13 and U15

2.4.2. On footprints for U9-U13 and U15 short pin 1 to pin 3, pin 4 to pin 6, pin 8 to pin 10 and pin 11 to pin 13

2.4.3. Reprogram U1-U6 with file “**PulseGenerator.jed**” dated 1/17/2002 7:22pm and U7 with file “**PulseGenControl.jed**” dated 1/13/2003 6:49pm, using instructions outlined in 2.3 CPLD programming and substituting these files.

2.4.4. Rework example



2.4 Counter Channel Test

2.4.1. Plug test board connector P1 into backplane.

2.4.2. Plug board under test connector P1 into backplane.

2.4.3. Using ribbon cable connector, connect P2 on test board to P2 on board under test.

2.4.4. Turn on power supply.

2.4.5. Open 5 Xterm windows on user interface Linux computer.

2.4.6. In Xterm window #1, type “rlogin aoicm –l ao” and hit return.

2.4.7. Type password “wai!mea” and hit return.

2.4.8. Type “su aroot” and hit return.

2.4.9. Type password “wai!mea” and hit return.

2.4.10. Change directory to “//manoaXX/lp” where XX is either 36 or 85 and hit return.

2.4.11. Type “start_ao” and hit return.

2.4.12. In Xterm window #2, type “rlogin aoicm –l ao” and hit return.

2.4.13. Type password “wai!mea” and hit return.

2.4.14. Change directory to “//manoaXX/ic” where XX is either 36 or 85 and hit return.

2.4.15. Type “ic” and hit return.

2.4.16. In Xterm window #3, type “rlogin aoicm –l ao” and hit return.

2.4.17. Type password “wai!mea” and hit return.

2.4.18. Change directory to “//manoaXX/socketio” where XX is either 36 or 85 and hit return.

2.4.19. Type “sock_server” and hit return.

2.4.20. In Xterm window #4, change directory to “//manoaXX/socketio” where XX is either 36 or 85 and hit return.

2.4.21. Type “sock_client” and hit return.

2.4.22. In Xterm window #5, change directory to “//manoaXX/xui” where XX is either 36 or 85 and hit return.

2.4.23. Type “xui” and hit return.

2.4.24. When the GUI pops up, click on the tab labeled “view”.

2.4.25. Click the radial button labeled “text”

2.4.26. Set SW1[8:6] to “011” and SW1[5:1] to “00000”.

2.4.27. Check to see that the first 24 channels all have the correct value as set on the test board using SW1. See following tables for function and rate of counts as set by SW1.

SW1[8:6]	Function
000	No counts, all outputs constant ‘0’
001	Pulses only on low phase
010	Pulses only on high phase
011	Pulses on both phases
100	Pulses on both phases
101	Pulses on both phases

110	Pulses on both phases
111	Pulses on both phases

SW1[5:1]	Pulse Rate	Count with membrane =2000
00000	1 pulse every 60ns	4380-4395
00001	1 pulse every 100ns	2630-2640
00010	1 pulse every 180ns	1460-1470
00011	1 pulse every 340ns	770-780
00100	1 pulse every 660ns	395-400
00101	1 pulse every 1.3us	200-205
00110	1 pulse every 2.58us	100-105
00111	1 pulse every 5.14us	50-55
01000	1 pulse every 10.26us	25-30
01001	1 pulse every 20.5us	10-15
01010	1 pulse every 40.98us	5-8
01011	1 pulse every 81.94us	2-5
01100	1 pulse every 163.86us	1-2
01101	1 pulse every 327.7us	0-1
01110	1 pulse every 655.38us	0-1
01111	1 pulse every 1310.72us	0-1
Else	1 pulse every 80ns	3115-3130

*Note that counts with membrane = 2000 are approximations, this number may differ depending on the on board oscillator and also upon the rate the multifunction board puts out phase. If pulses are expected on both phases, high counts and low counts may be slightly different, but should be around the same value.

2.4.28. Change SW[8:6] to “001” and check to see that you only get low counts are in the correct range and that the high count is ‘0’ or nearly to ‘0’.

2.4.29. Change SW[8:6] to “010” and check to see that you only get high counts are in the correct range and that the low count is ‘0’ or nearly to ‘0’.

2.4.30. Change SW[8:6] back to “011” and change SW[5:1] to “00001” and make sure that you get counts on both phases and that the counts are in the correct range.

2.4.31. Change SW[5:1] to next value in table and check that counts are in correct range.

2.4.32. Repeat previous step for all values in table.

2.4.33. Change SW1[8:6] on board under test and make sure that board can be addressed properly in all valid address ranges. See table from section 1.7 for address ranges and values.

2.4.34. Right click on “Quit” in GUI.

2.4.35. Move curser over Xterm #4 and press cntrl-c.

2.4.36. Move curser over Xterm #3 and press cntrl-c.

2.4.37. Move curser over Xterm #2 and press cntrl-c.

2.4.38. Turn off power supply.

2.4.39. Remove board.

2.4.40. If there are more boards to test, insert board into backplane and turn power on.

2.4.41. In Xterm #1, type “stop_ao” and hit return.

2.4.42. In Xterm #1, type “start_ao” and hit return.

2.4.43. In Xterm #2, type “ic” and hit return.

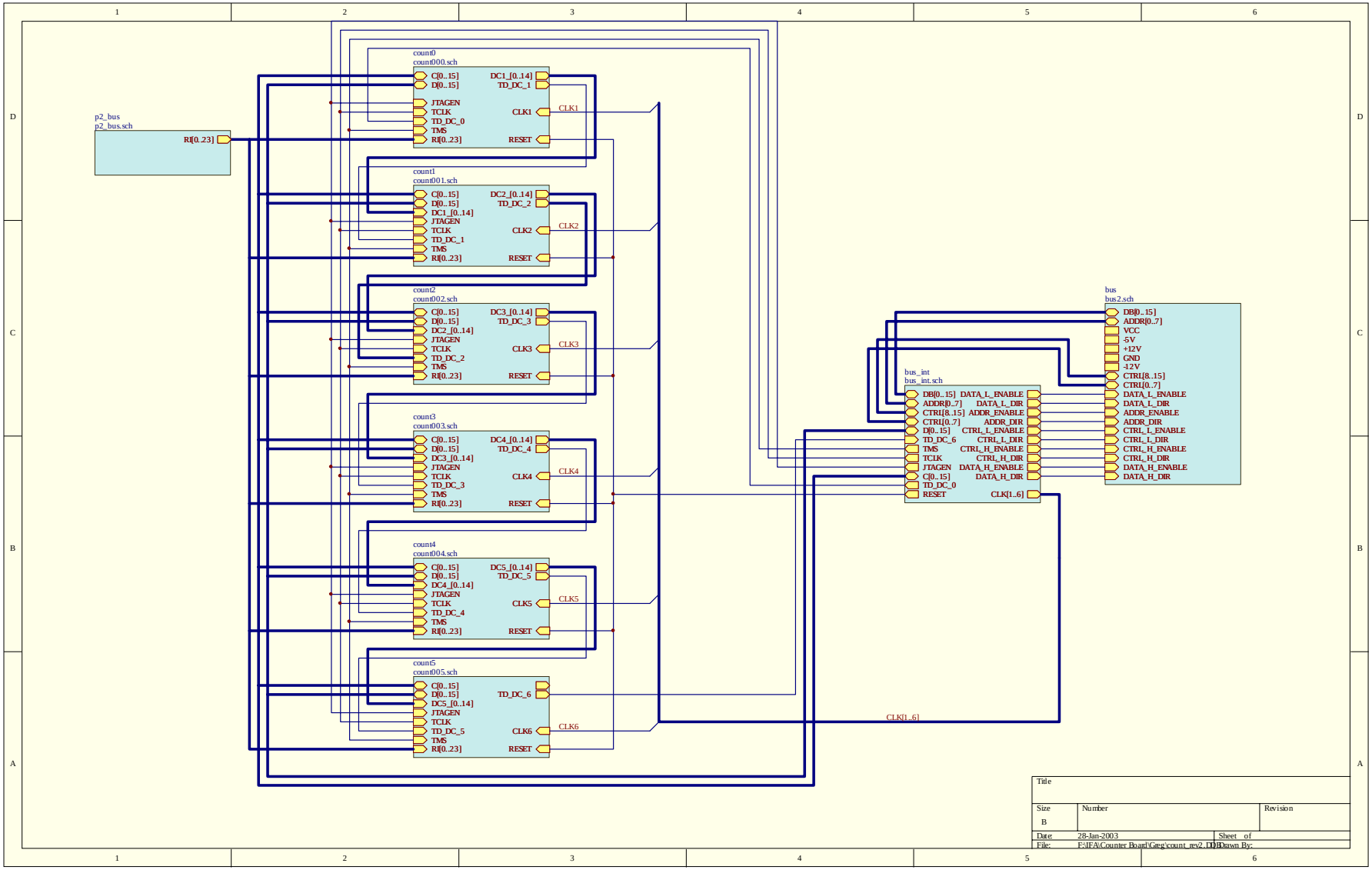
2.4.44. In Xterm #3, type “sock_server” and hit return.

2.4.45. In Xterm #4, type “sock_client” and hit return.

2.4.46. In Xterm #5, type “xui” and hit return.

2.4.47. Repeat from step 2.4.24.

3 Schematic



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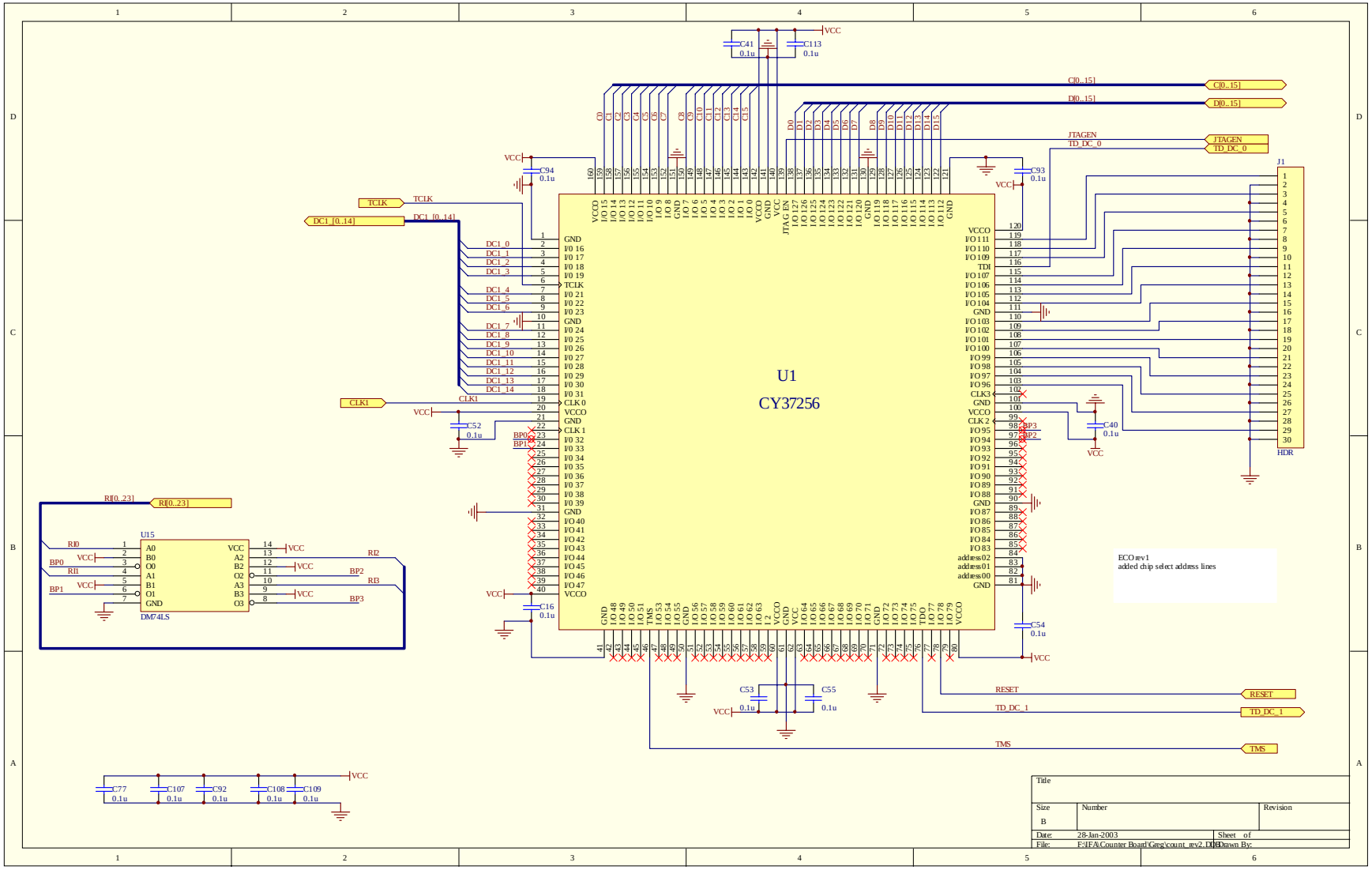

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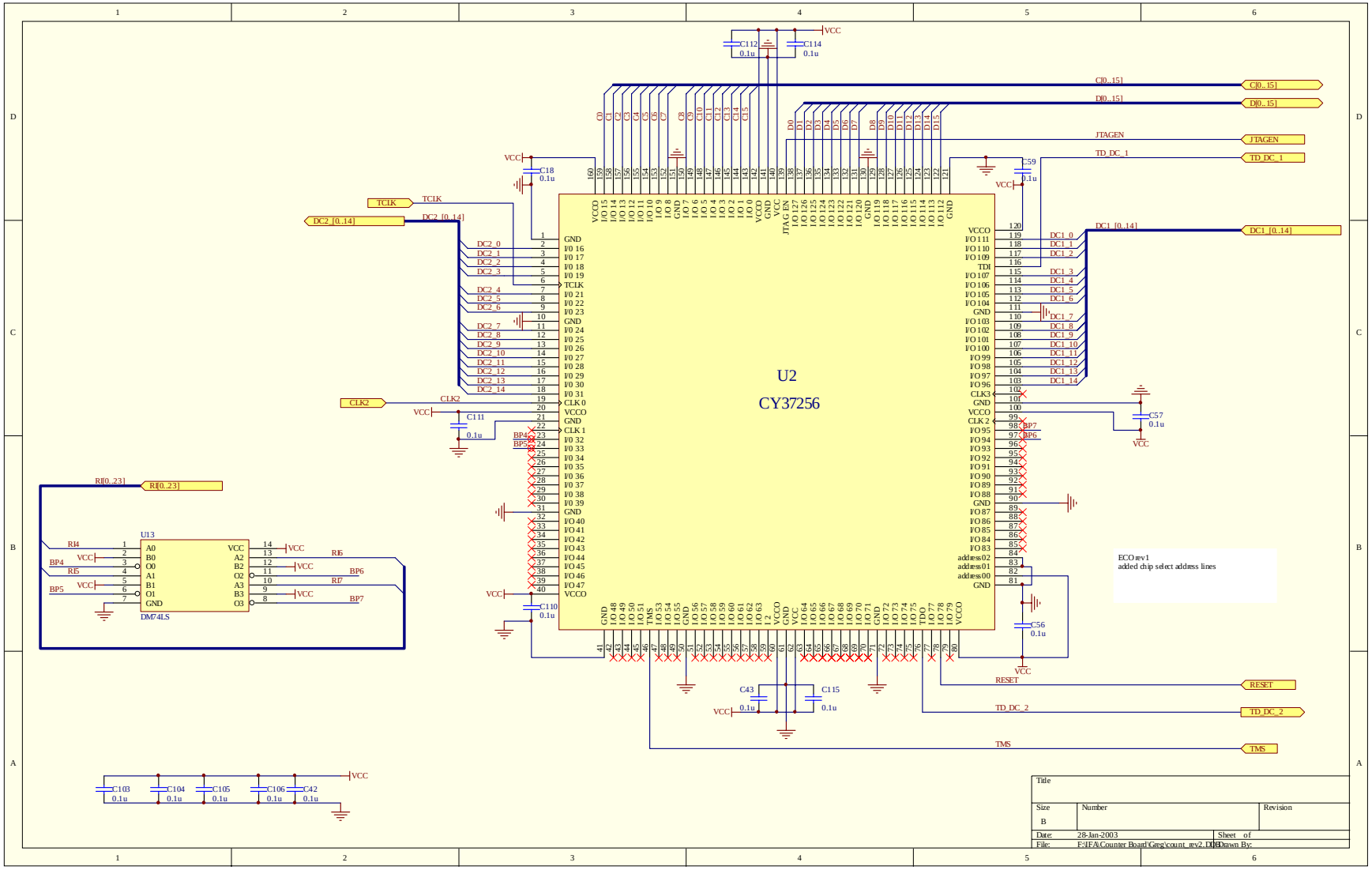
Counter Board



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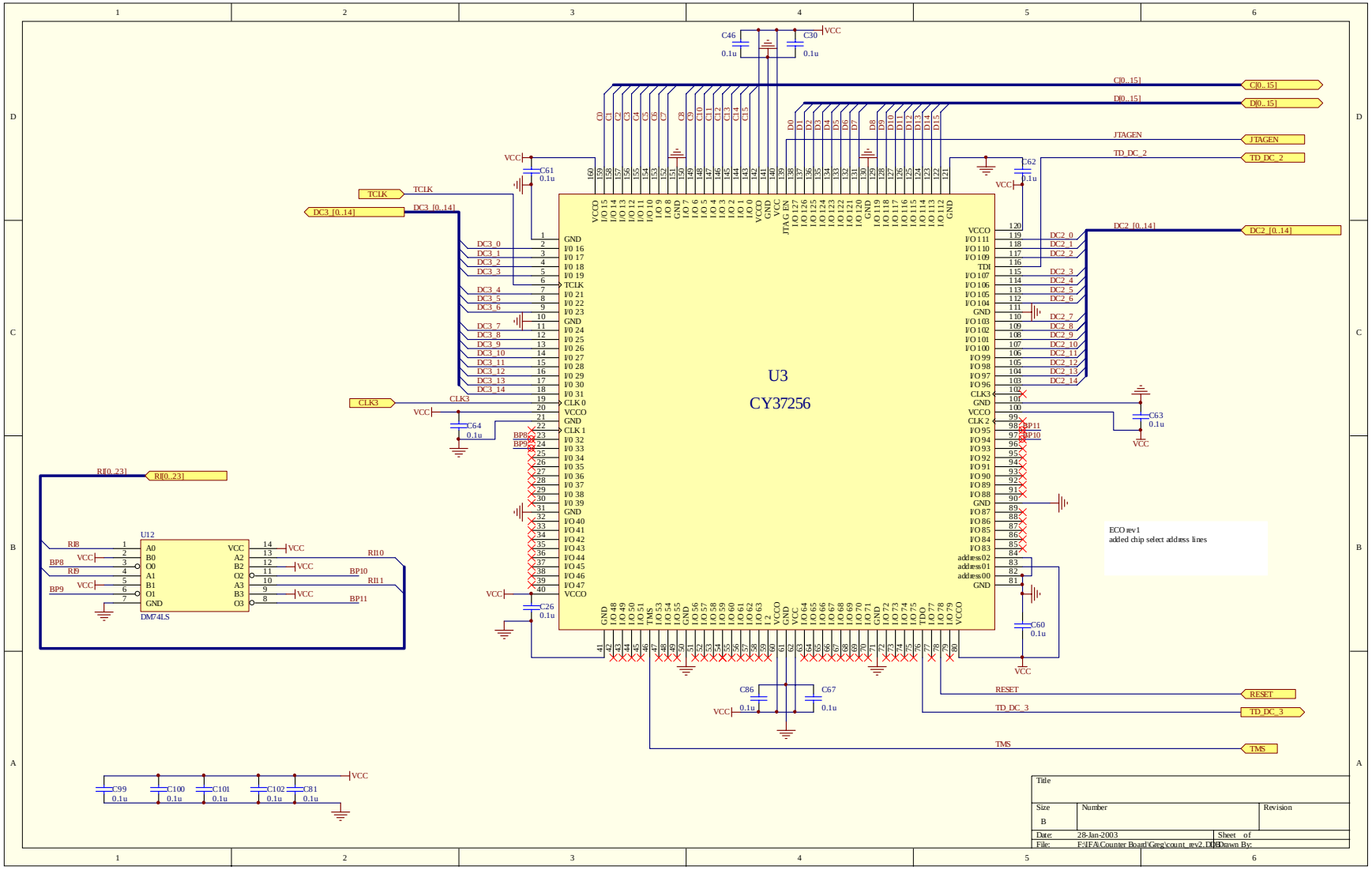

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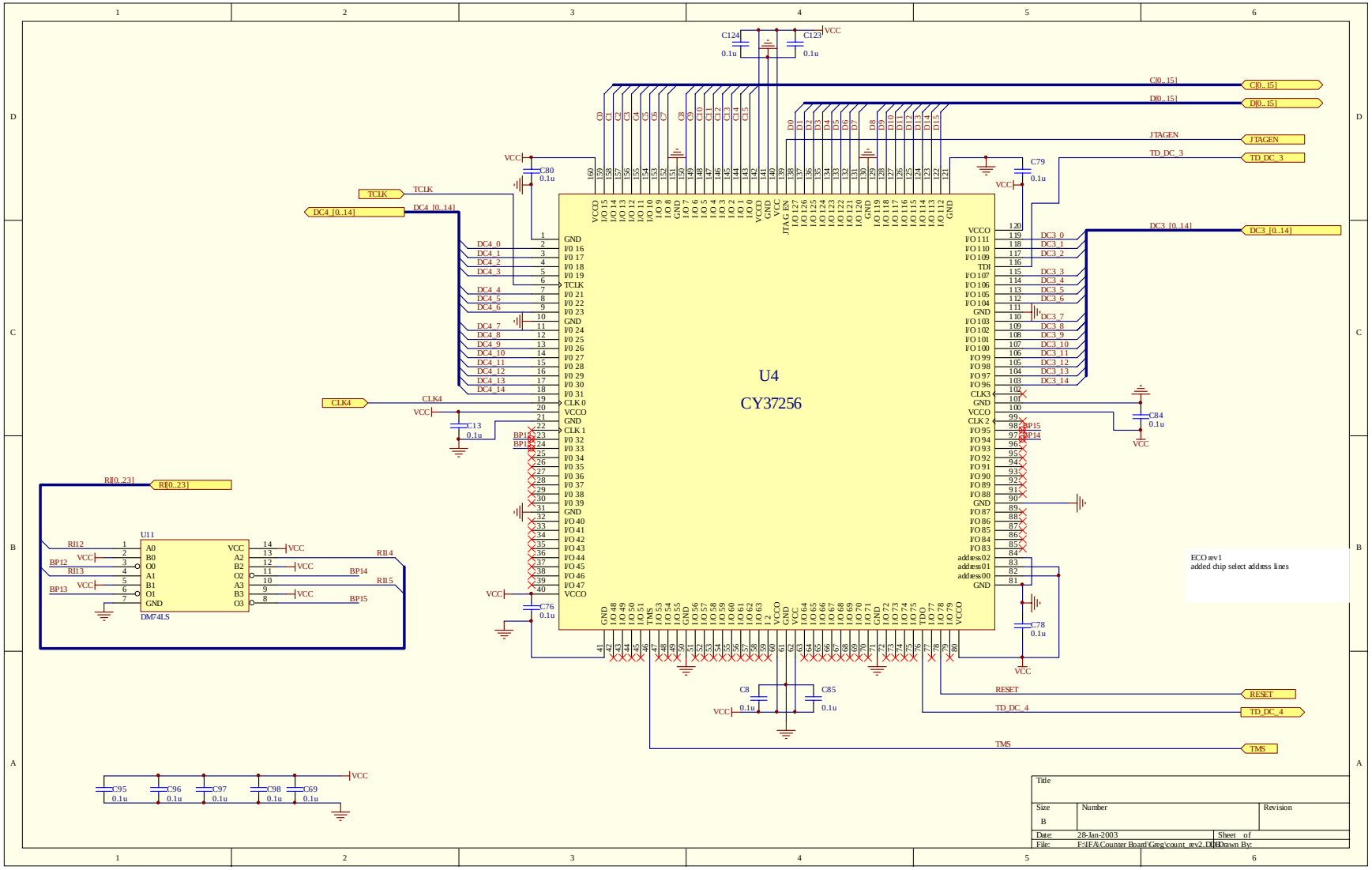

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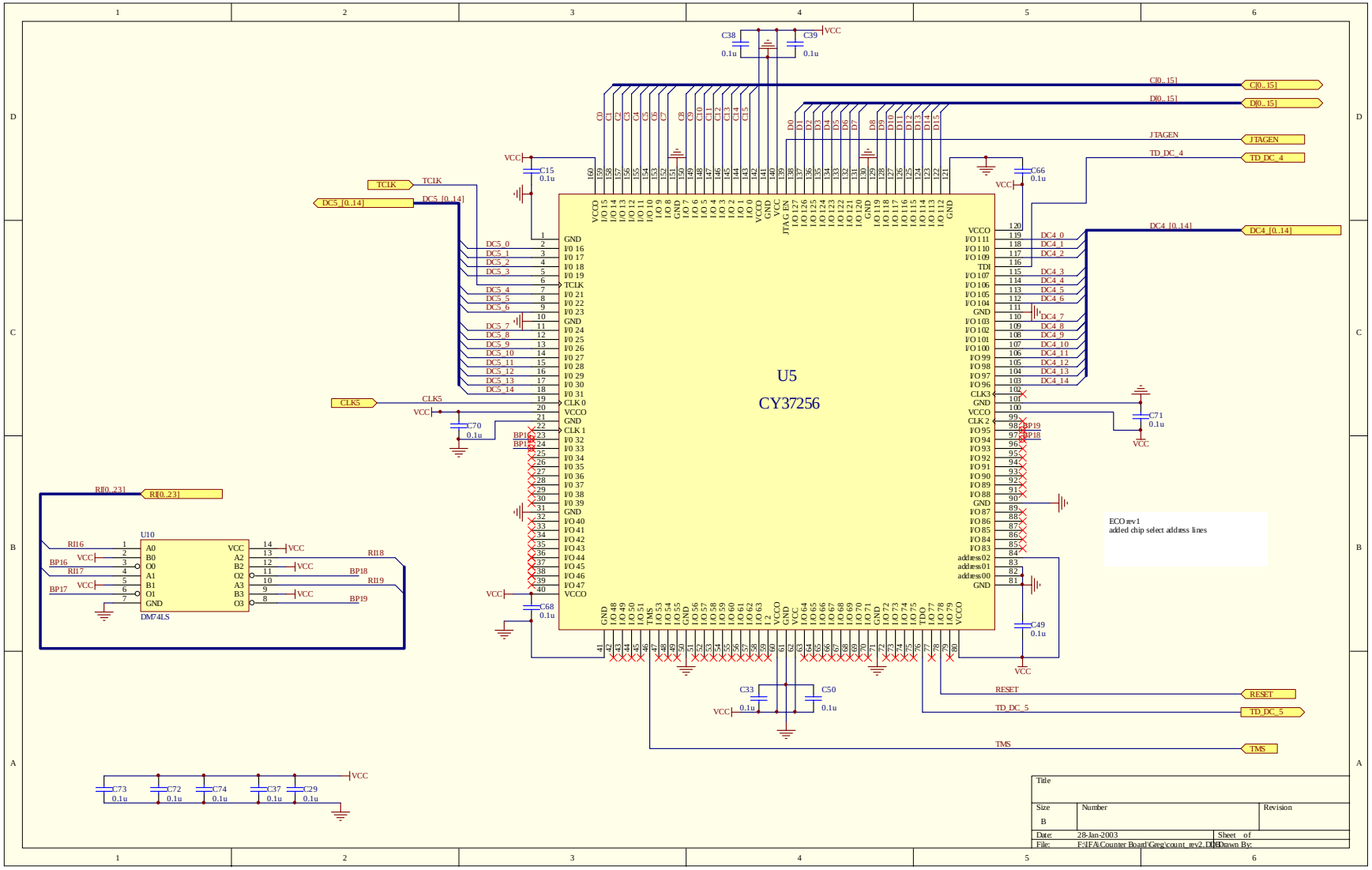

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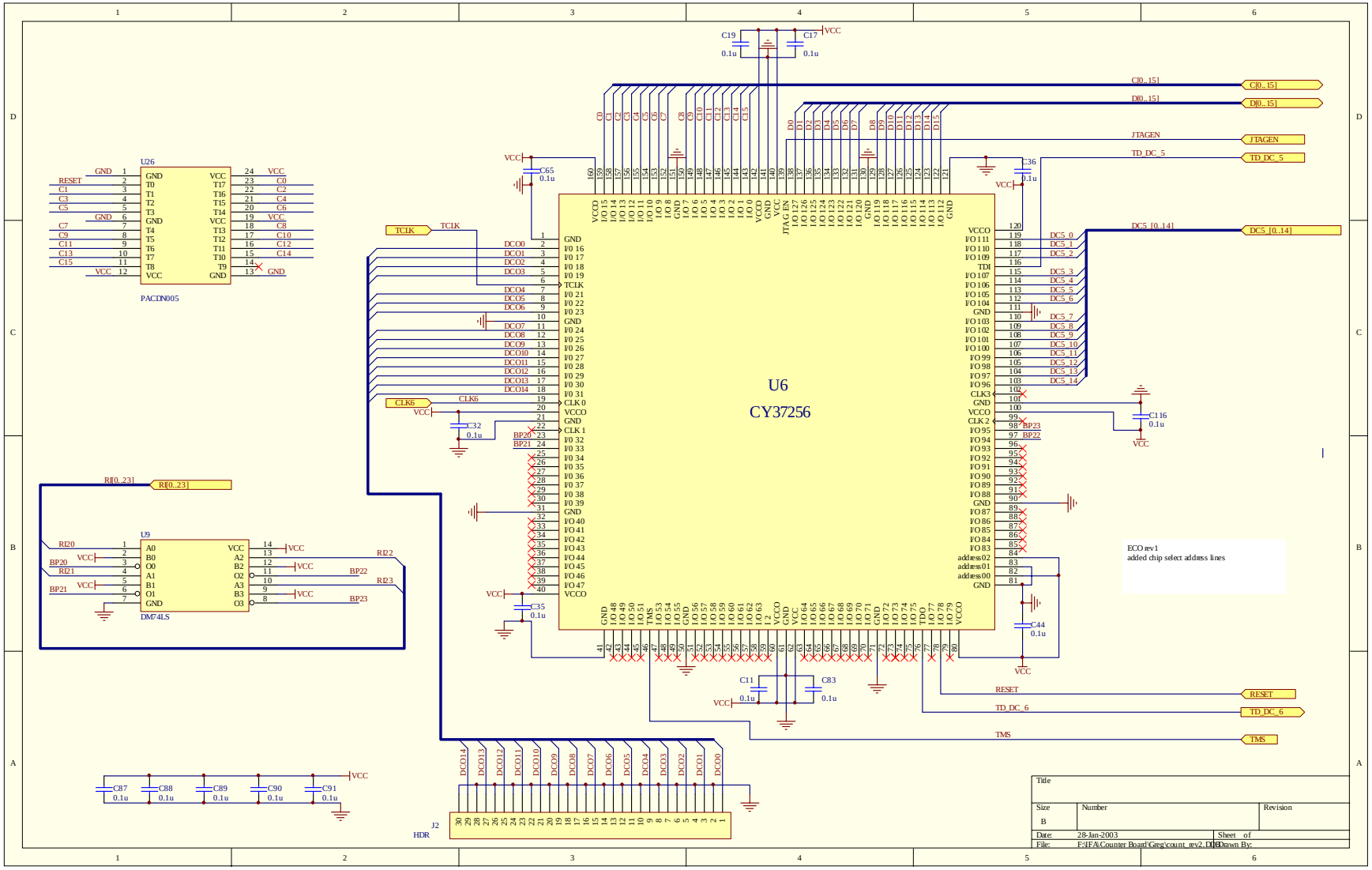

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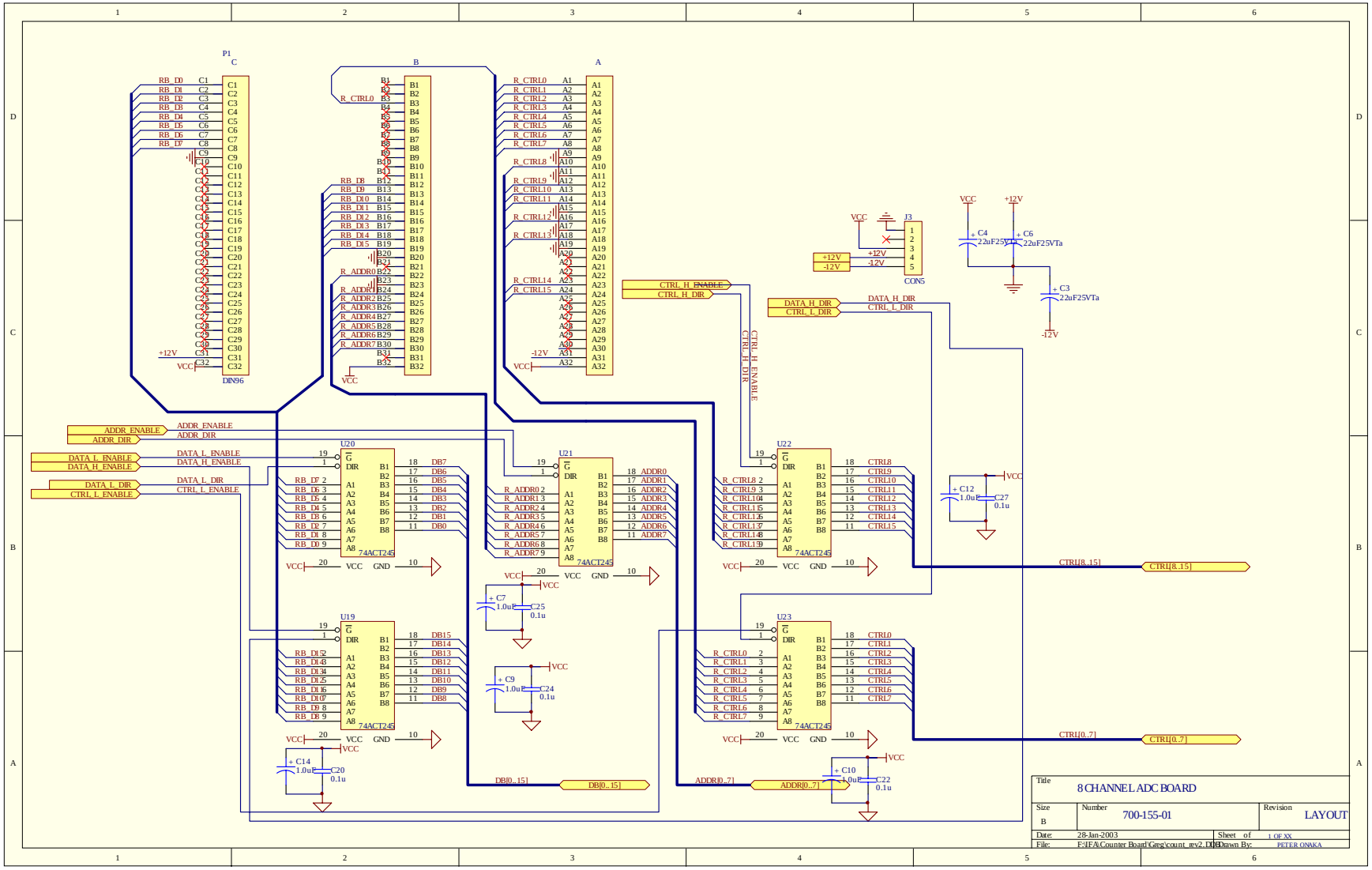

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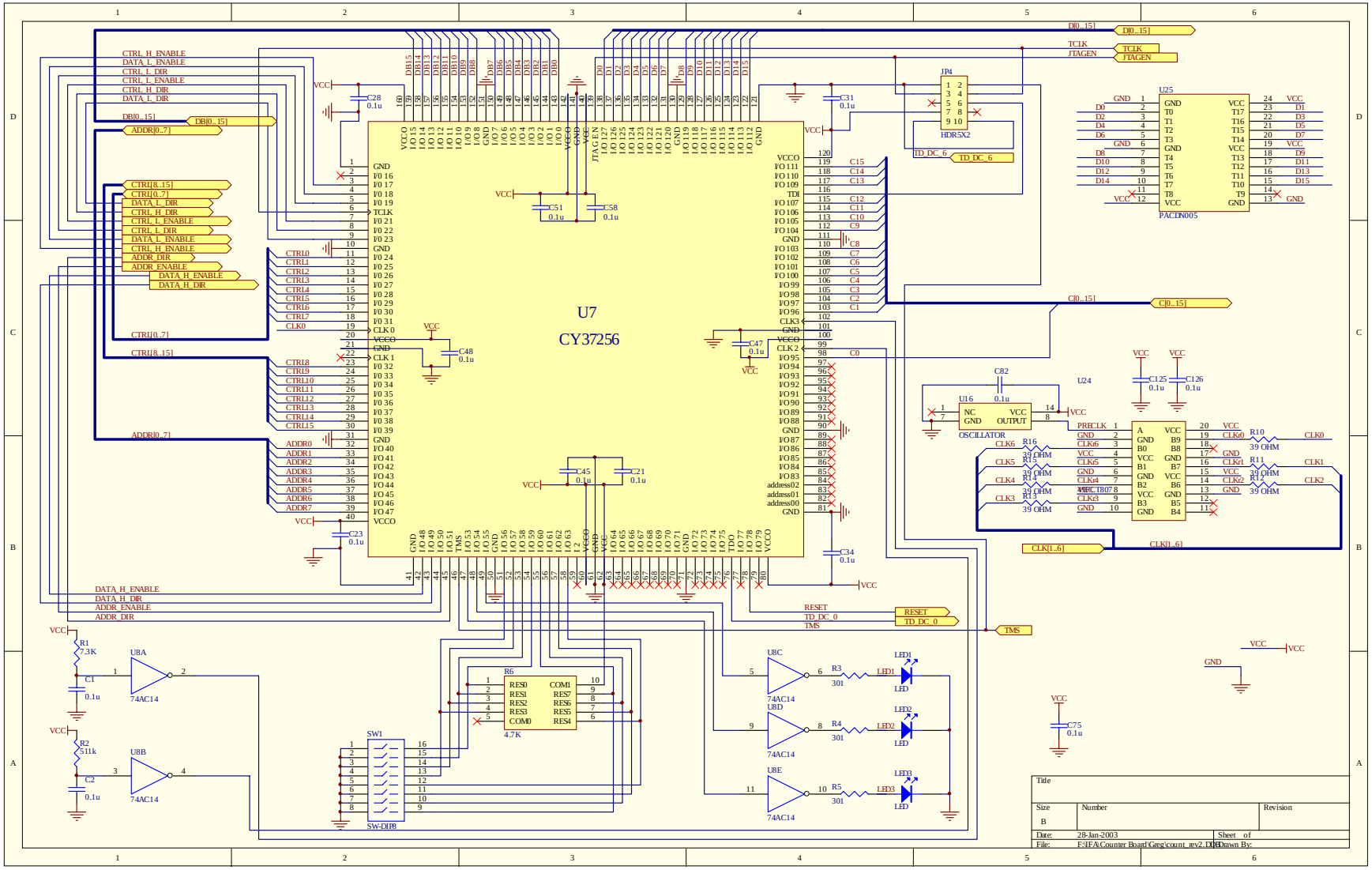

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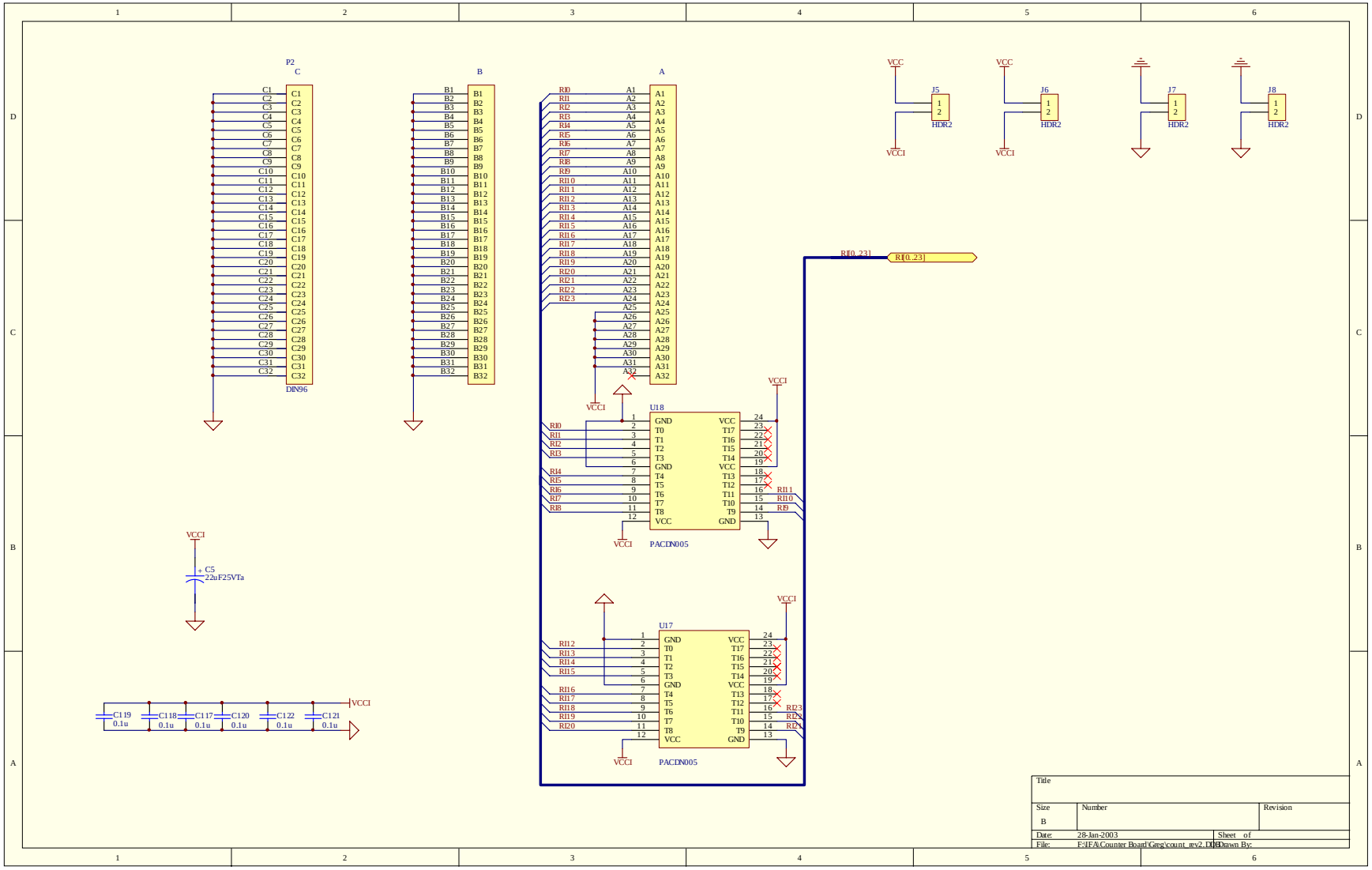

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4 VHDL Code

4.1 Control Chip

```
--modified by Peter Onaka
--  This is the top level of the control chip for the counter Board.
--
--************************************************************
--  Revision history
--
--  Date        Rev Eng             Description
--  --------    --- --------------  ---------------------
--  11/30/02    1   RY              Initial File
--  12/24/02    2   PMO             changed tristate signals
--  12/27/02    3   PMO             added bp_reset to c6
--  01/02/03    4   RY              changed unused Control lines to highZ instead of driving '0' a
--                                  commented out debug lines
--  01/02/03    5   RY              swapped pins 42 and 43 in the control file because they are sw
--                                  on the board.
--  01/02/03    6   RY              Changed polarity of clock for outputing address to counter chi
--                                  Counter chips clock Address in on rising edge so adress should
--                                  clocked out on falling edge.

library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity Control_Top is
    port(
        LED :               out std_logic_vector(3 downto 1);
        SYSCLK:             in STD_LOGIC;
        --
        -- backplane data bus and associated control signal
        --
        BPADDR:             in std_logic_vector(7 downto 0);
        BPCTRL:             in std_logic_vector(15 downto 0);
        BPD:                out std_logic_vector(15 downto 0);
        BPD_L_TRISTATE:     out std_logic;
        BPD_H_TRISTATE:     out std_logic;
        bpd_h_dir:          out std_logic;
        bpd_l_dir:          out std_logic;
        bpaddr_dir:         out std_logic;
        bpaddr_tristate:    out std_logic;
        bpctrl_h_dir:       out std_logic;
        bpctrl_l_dir:       out std_logic;
        bpctrl_h_tristate:  out std_logic;
        bpctrl_l_tristate:  out std_logic;
        SW:                 in std_logic_vector(7 downto 0);
        --
        -- internal bus
        --
        D:                  in std_logic_vector(15 downto 0);
        C:                  out std_logic_vector(15 downto 0)
    );
end Control_Top;

architecture Control_Top of Control_Top is
    signal Addr_rising:     STD_LOGIC_VECTOR(7 downto 0); -- stores the address at the rising edge
    signal Addr_Valid:      STD_LOGIC; -- Address is stable for 2 consectutive clock edges
    signal Addr_Good:       STD_LOGIC; -- Address is on board
begin
    -- constant signals
    C(15 downto 8)  <= (others => 'Z');
    bpd_h_dir <= '0';
    bpd_l_dir <= '0';
    bpaddr_dir <= '1';
    bpaddr_tristate <= '0';
    bpctrl_h_dir <= '0';
    bpctrl_l_dir <= '1';
    bpctrl_h_tristate <= '1';
    bpctrl_l_tristate <= '0';
    LED <= "000";

    -- validate back plane address
    valid_Addr : process(SYSCLK, Addr_rising, BPADDR)
    begin
        -- Store BP adress at rising clock edge for comparison to BP address at falling clock edge
```

```
        -- Create half clock cycle delayed version of Addr_Valid
        if (SYSCLK'event and SYSCLK = '1') then
            Addr_rising <= BPADDR(7 downto 0);
            if (Addr_rising = BPADDR) then
                Addr_Valid <= '1';
            else
                Addr_Valid <= '0';
            end if;
        end if;
        -- check if BP address is stable on falling clock edge
--      if (SYSCLK'event and SYSCLK = '0') then
--          -- if BP adress is stable then Addr_Valid = '1'
--          if (Addr_rising = BPADDR) then
--              Addr_Valid <= '1';
--          -- if BP address is NOT stable then Addr_Valid = '0'
--          else
--              Addr_Valid <= '0';
--          end if;
--      end if;
    end process;

    -- drive BP_Tristates when Address is valid and Upper Address matches SW[7:5]
    -- Create Output Enable signal for Counter chips
    control7 : process (Addr_Valid, Addr_Good)
    begin
        if (Addr_Valid = '1') and (Addr_Good = '1') then
            C(7) <= '1';
            BPD_L_TRISTATE <=  '0';-- was'1';
            BPD_H_TRISTATE <= '0';-- was '1';
        else
            C(7) <= '0';
            BPD_L_TRISTATE <=  '1'; --was '0';
            BPD_H_TRISTATE <= '1'; --was '0';
        end if;
    end process;
-- DEBUG --
--  C(8) <= Addr_Valid;
--  C(9) <= Addr_Good;
-- END DEBUG --
-- missing reset signal PMO
    C(6) <= BPCTRL(3);
    -- Pass Data and phase directly out
    BPD(15 downto 0) <= D(15 downto 0);
    C(0) <= BPCTRL(1);

    -- pass BP address to counter chips and set Addr_Good = '1' if it matches SW
    -- else pass all ones and set Addr_Good = '0'
    board_addr : process(SYSCLK, BPADDR, SW)
    begin
        if (SYSCLK'event and SYSCLK = '0') then
            -- if BP address is on board then set address bits to BPAddr and Addr_Good = '1'
            if (BPADDR(7 downto 5) = SW(7 downto 5)) then
                C(5 downto 1) <= BPADDR(4 downto 0);
                Addr_Good <= '1';
            -- if BP address is not on board then set address bits to all ones and Addr_Good = '0'
            else
                C(5 downto 1) <= "11111";
                Addr_Good <= '0';
            end if;
        end if;
    end process;


end Control_Top;
```

```
---
-- Digital to analog converter control lines
--
--
-- Bus Address control
--
Attribute PIN_NUMBERS of bpctrl_h_tristate is   "3";
Attribute PIN_NUMBERS of bpd_l_tristate is  "4";
Attribute PIN_NUMBERS of bpctrl_l_dir is    "5";
--
-- Bus Data control
--
Attribute PIN_NUMBERS of bpctrl_l_tristate is   "7";
Attribute PIN_NUMBERS of bpctrl_h_dir is    "8";
Attribute PIN_NUMBERS of bpd_l_dir is       "9";
--
-- Bus Ctrl signals
Attribute PIN_NUMBERS of bpctrl(0) is       "11";
Attribute PIN_NUMBERS of bpctrl(1) is       "12";
Attribute PIN_NUMBERS of bpctrl(2) is       "13";
Attribute PIN_NUMBERS of bpctrl(3) is       "14";
Attribute PIN_NUMBERS of bpctrl(4) is       "15";
Attribute PIN_NUMBERS of bpctrl(5) is       "16";
Attribute PIN_NUMBERS of bpctrl(6) is       "17";
Attribute PIN_NUMBERS of bpctrl(7) is       "18";
Attribute PIN_NUMBERS of bpctrl(8) is       "23";
Attribute PIN_NUMBERS of bpctrl(9) is       "24";
Attribute PIN_NUMBERS of bpctrl(10) is      "25";
Attribute PIN_NUMBERS of bpctrl(11) is      "26";
Attribute PIN_NUMBERS of bpctrl(12) is      "27";
Attribute PIN_NUMBERS of bpctrl(13) is      "28";
Attribute PIN_NUMBERS of bpctrl(14) is      "29";
Attribute PIN_NUMBERS of bpctrl(15) is      "30";
--
-- Power up pins attached to r/c timers
--
Attribute PIN_NUMBERS of SYSCLK is          "19";
--
-- Bus address signals
--
Attribute PIN_NUMBERS of bpaddr(0) is       "32";
Attribute PIN_NUMBERS of bpaddr(1) is       "33";
Attribute PIN_NUMBERS of bpaddr(2) is       "34";
Attribute PIN_NUMBERS of bpaddr(3) is       "35";
Attribute PIN_NUMBERS of bpaddr(4) is       "36";
Attribute PIN_NUMBERS of bpaddr(5) is       "37";
Attribute PIN_NUMBERS of bpaddr(6) is       "38";
Attribute PIN_NUMBERS of bpaddr(7) is       "39";

--
-- Bus control control
--
Attribute PIN_NUMBERS of bpd_h_dir is       "43";
Attribute PIN_NUMBERS of bpd_h_tristate is  "42";
Attribute PIN_NUMBERS of bpaddr_tristate is "44";
Attribute PIN_NUMBERS of bpaddr_dir is      "45";
--
-- Lines driving LED's
--
Attribute PIN_NUMBERS of led(1) is    "47";
Attribute PIN_NUMBERS of led(2) is        "48";
Attribute PIN_NUMBERS of led(3) is        "49";
--
-- Address switch lines
--
Attribute PIN_NUMBERS of sw(3) is        "51";
Attribute PIN_NUMBERS of sw(2) is        "52";
Attribute PIN_NUMBERS of sw(1) is        "53";
Attribute PIN_NUMBERS of sw(0) is        "54";
Attribute PIN_NUMBERS of sw(7) is        "55";
Attribute PIN_NUMBERS of sw(6) is        "56";
Attribute PIN_NUMBERS of sw(5) is        "57";
Attribute PIN_NUMBERS of sw(4) is        "58";
```

```
 74
 75 Attribute PIN_NUMBERS of RESET_CNT is        "78";
 76
 77 Attribute PIN_NUMBERS of c(0) is    "98"; -- Not available on 192 version.
 78 Attribute PIN_NUMBERS of c(1) is    "103";
 79 Attribute PIN_NUMBERS of c(2) is    "104";
 80 Attribute PIN_NUMBERS of c(3) is    "105";
 81 Attribute PIN_NUMBERS of c(4) is    "106";
 82 Attribute PIN_NUMBERS of c(5) is    "107";
 83 Attribute PIN_NUMBERS of c(6) is    "108";
 84 Attribute PIN_NUMBERS of c(7) is    "109";
 85 Attribute PIN_NUMBERS of c(8) is    "110";
 86 Attribute PIN_NUMBERS of c(9) is    "112";
 87 Attribute PIN_NUMBERS of c(10) is   "113";
 88 Attribute PIN_NUMBERS of c(11) is   "114";
 89 Attribute PIN_NUMBERS of c(12) is   "115";
 90 Attribute PIN_NUMBERS of c(13) is   "117";
 91 Attribute PIN_NUMBERS of c(14) is   "118";
 92 Attribute PIN_NUMBERS of c(15) is   "119";
 93
 94 Attribute PIN_NUMBERS of d(15) is   "122"; -- Not available on 192 version.
 95 Attribute PIN_NUMBERS of d(14) is   "123";
 96 Attribute PIN_NUMBERS of d(13) is   "124";
 97 Attribute PIN_NUMBERS of d(12) is   "125";
 98 Attribute PIN_NUMBERS of d(11) is   "126";
 99 Attribute PIN_NUMBERS of d(10) is   "127";
100 Attribute PIN_NUMBERS of d(9) is    "128";
101 Attribute PIN_NUMBERS of d(8) is    "129";
102 Attribute PIN_NUMBERS of d(7) is    "131";
103 Attribute PIN_NUMBERS of d(6) is    "132";
104 Attribute PIN_NUMBERS of d(5) is    "133";
105 Attribute PIN_NUMBERS of d(4) is    "134";
106 Attribute PIN_NUMBERS of d(3) is    "135";
107 Attribute PIN_NUMBERS of d(2) is    "136";
108 Attribute PIN_NUMBERS of d(1) is    "137";
109 Attribute PIN_NUMBERS of d(0) is    "138";
110
111 --
112 -- Bus data signals
113 --
114 Attribute PIN_NUMBERS of bpd(0) is  "143";
115 Attribute PIN_NUMBERS of bpd(1) is  "144";
116 Attribute PIN_NUMBERS of bpd(2) is  "145";
117 Attribute PIN_NUMBERS of bpd(3) is  "146";
118 Attribute PIN_NUMBERS of bpd(4) is  "147";
119 Attribute PIN_NUMBERS of bpd(5) is  "148";
120 Attribute PIN_NUMBERS of bpd(6) is  "149";
121 Attribute PIN_NUMBERS of bpd(7) is  "150";
122 Attribute PIN_NUMBERS of bpd(8) is  "152";
123 Attribute PIN_NUMBERS of bpd(9) is  "153";
124 Attribute PIN_NUMBERS of bpd(10) is "154";
125 Attribute PIN_NUMBERS of bpd(11) is "155";
126 Attribute PIN_NUMBERS of bpd(12) is "156";
127 Attribute PIN_NUMBERS of bpd(13) is "157";
128 Attribute PIN_NUMBERS of bpd(14) is "158";
129 Attribute PIN_NUMBERS of bpd(15) is "159";
130
131
132
133
134
```

4.2 Counter Chip

```
1  --
2  --  Counter Board Counter chip
3  --
4  --  ************************************************************
5  --  Revision history
6  --
7  --  Date        Rev Eng             Description
8  --  --------    --- --------------  ---------------------
9  --  12/16/02    1   RY              Initial File
10 --  12/27/02    2   PMO             changed reset polarity
11 --  12/31/02    3   RY              OE does  not rely on C(7)
12 --  12/31/02    4   RY              added testpoint for output enable to pin 48
13 --  12/31/02    5   RY              commented out everything that was added, should be same as Rev
14 --  1/3/2002    7?  PMO             try to sync APD input, C(0) sync fixed problem
15 library IEEE;
16 use IEEE.std_logic_1164.all;
17
18 entity Counter is
19     port (
20         SYSCLK:         in STD_LOGIC;
21         C:              in STD_LOGIC_VECTOR(7 downto 0);
22         DCI:            in STD_LOGIC_VECTOR(2 downto 0);
23         COUNT_SIGNAL:   in STD_LOGIC_VECTOR(4 downto 1);
24         D:              out STD_LOGIC_VECTOR(15 downto 0);
25 -- debug
26         OUTEN:          out STD_LOGIC;
27 -- end debug
28         DCO:            out STD_LOGIC_VECTOR(2 downto 0)
29         );
30 end Counter;
31
32 architecture Counter of Counter is
33 --  signal TempCount:   STD_LOGIC_VECTOR(13 downto 0);
34 --  signal TempCount1:  STD_LOGIC_VECTOR(13 downto 0);
35 --  signal HighCountA:  STD_LOGIC_VECTOR(13 downto 0);
36 --  signal LowCountA:   STD_LOGIC_VECTOR(13 downto 0);
37 --  signal HighCountB:  STD_LOGIC_VECTOR(13 downto 0);
38 --  signal LowCountB:   STD_LOGIC_VECTOR(13 downto 0);
39 --  signal HighCountC:  STD_LOGIC_VECTOR(13 downto 0);
40 --  signal LowCountC:   STD_LOGIC_VECTOR(13 downto 0);
41 --  signal HighCountD:  STD_LOGIC_VECTOR(13 downto 0);
42 --  signal LowCountD:   STD_LOGIC_VECTOR(13 downto 0);
43     signal TempCount:   STD_LOGIC_VECTOR(14 downto 0);
44     signal TempCount1:  STD_LOGIC_VECTOR(14 downto 0);
45     signal HighCountA:  STD_LOGIC_VECTOR(14 downto 0);
46     signal LowCountA:   STD_LOGIC_VECTOR(14 downto 0);
47     signal HighCountB:  STD_LOGIC_VECTOR(14 downto 0);
48     signal LowCountB:   STD_LOGIC_VECTOR(14 downto 0);
49     signal HighCountC:  STD_LOGIC_VECTOR(14 downto 0);
50     signal LowCountC:   STD_LOGIC_VECTOR(14 downto 0);
51     signal HighCountD:  STD_LOGIC_VECTOR(14 downto 0);
52     signal LowCountD:   STD_LOGIC_VECTOR(14 downto 0);
53     signal Pre_Out_En:  STD_LOGIC;
54     signal Output_En:   STD_LOGIC;
55     signal Phase_Not:   STD_LOGIC;
56     signal Reset_Low:   STD_LOGIC;
57     signal Reset_High:  STD_LOGIC;
58     signal pulse_out1:  STD_LOGIC; --PMO
59     signal sync_out1:   STD_LOGIC; --PMO
60     signal pulse_out2:  STD_LOGIC; --PMO
61     signal sync_out2:   STD_LOGIC; --PMO
62     signal pulse_out3:  STD_LOGIC; --PMO
63     signal sync_out3:   STD_LOGIC; --PMO
64     signal pulse_out4:  STD_LOGIC; --PMO
65     signal sync_out4:   STD_LOGIC; --PMO
66     signal C0_sync: STD_LOGIC; --PMO
67     signal COUNT_SIG1:  STD_LOGIC; --PMO
68     signal COUNT_SIG2:  STD_LOGIC; --PMO
69     signal COUNT_SIG3:  STD_LOGIC; --PMO
70     signal COUNT_SIG4:  STD_LOGIC; --PMO
71     signal c6_sync: STD_LOGIC; --PMO
72
73 -- instantiate sync_Counter
```

```
 74
 75 component sync_Counter -- is
 76         port (
 77             RESET:      in STD_LOGIC;
 78             COUNT_EN:   in STD_LOGIC;
 79             D_IN:    in STD_LOGIC;
 80             clk:     in STD_LOGIC;
 81 --          COUNT_OUT:  out STD_LOGIC_VECTOR(13 downto 0)
 82             COUNT_OUT:  out STD_LOGIC_VECTOR(14 downto 0)
 83             );
 84     end component; --sync_Counter;
 85
 86 begin
 87
 88     sync_phase : process  (SYSCLK)
 89     begin
 90     if (SYSCLK'event and SYSCLK = '1') then
 91         C0_sync <= C(0);
 92         c6_sync <= C(6);
 93     end if;
 94     end process;
 95
 96     Phase_Not   <= not(C0_sync);
 97     Reset_High  <= c6_sync and Phase_Not;
 98     Reset_Low   <= c6_sync and C0_sync;
 99 --  Reset_High  <= C(6) and Phase_Not;
100 --  Reset_Low   <= C(6) and C0_sync;
101     -- create inverted phase, reset
102
103
104     addr_decode : process
105     begin
106             -- if upper address bits match DCI then output data
107             if (C(5 downto 3) = DCI(2 downto 0)) then
108                 -- select which count to output
109                 case (C(2 downto 1)) is
110                     when "00" =>
111                         if C0_sync = '0' then
112                             TempCount <= HighCountA;
113                         else
114                             TempCount <= LowCountA;
115                         end if;
116                     when "01" =>
117                         if C0_sync = '0' then
118                             TempCount <= HighCountB;
119                         else
120                             TempCount <= LowCountB;
121                         end if;
122                     when "10" =>
123                         if C0_sync = '0' then
124                             TempCount <= HighCountC;
125                         else
126                             TempCount <= LowCountC;
127                         end if;
128                     when "11" =>
129                         if C0_sync = '0' then
130                             TempCount <= HighCountD;
131                         else
132                             TempCount <= LowCountD;
133                         end if;
134                     when others =>
135                 end case;
136             end if;
137     end process;
138
139
140     next_addr : process (DCI)
141     begin
142         case (DCI(2 downto 0)) is
143             -- '000' next address '001'
144             when "000" => DCO(2 downto 0) <= "001";
145             -- '001' next address '010'
146             when "001" => DCO(2 downto 0) <= "010";
```

```
147             -- '010' next address '011'
148             when "010" => DCO(2 downto 0) <= "011";
149             -- '011' next address '100'
150             when "011" => DCO(2 downto 0) <= "100";
151             -- '100' next address '101'
152             when "100" => DCO(2 downto 0) <= "101";
153             when others => DCO(2 downto 0) <= "000";
154         end case;
155     end process;
156 
157     -- First Counter
158     counterhighA : sync_Counter
159         port map(
160             RESET       => Reset_High,
161             COUNT_EN    => C0_sync,
162             D_IN    => sync_out1,
163             clk     => SYSCLK,
164             COUNT_OUT   => HighCountA
165             );
166     counterlowA : sync_Counter
167         port map(
168             RESET       => Reset_Low,
169             COUNT_EN    => Phase_Not,
170             D_IN    => sync_out1,
171             clk     => SYSCLK,
172             COUNT_OUT   => LowCountA
173             );
174     -- End First Counter
175 
176     -- Second Counter
177     counterhighB : sync_Counter
178         port map(
179             RESET       => Reset_High,
180             COUNT_EN    => C0_sync,
181             D_IN    => sync_out2,
182             clk     => SYSCLK,
183             COUNT_OUT   => HighCountB
184             );
185     counterlowB : sync_Counter
186         port map(
187             RESET       => Reset_Low,
188             COUNT_EN    => Phase_Not,
189             D_IN    => sync_out2,
190             clk     => SYSCLK,
191             COUNT_OUT   => LowCountB
192             );
193     -- End Second Counter
194 
195     -- Third Counter
196     counterhighC : sync_Counter
197         port map(
198             RESET       => Reset_High,
199             COUNT_EN    => C0_sync,
200             D_IN    => sync_out3,
201             clk     => SYSCLK,
202             COUNT_OUT   => HighCountC
203             );
204     counterlowC : sync_Counter
205         port map(
206             RESET       => Reset_Low,
207             COUNT_EN    => Phase_Not,
208             D_IN    => sync_out3,
209             clk     => SYSCLK,
210             COUNT_OUT   => LowCountC
211             );
212     -- End Third Counter
213 
214     -- Fourth Counter
215     counterhighD : sync_Counter
216         port map(
217             RESET       => Reset_High,
218             COUNT_EN    => C0_sync,
219             D_IN    => sync_out4,
```

```
220             clk     => SYSCLK,
221             COUNT_OUT   => HighCountD
222             );
223     counterlowD : sync_Counter
224         port map(
225             RESET       => Reset_Low,
226             COUNT_EN    => Phase_Not,
227             D_IN    => sync_out4,
228             clk     => SYSCLK,
229             COUNT_OUT   => LowCountD
230             );
231     -- End Fourth Counter
232
233 -- APD sync
234 -- invert COUNT_SIGNAL# s
235     COUNT_SIG1 <= not COUNT_SIGNAL(1);
236     COUNT_SIG2 <= not COUNT_SIGNAL(2);
237     COUNT_SIG3 <= not COUNT_SIGNAL(3);
238     COUNT_SIG4 <= not COUNT_SIGNAL(4);
239
240 --  pulse_APD1 : process (sysclk,COUNT_SIGNAL(1),sync_out1)
241 pulse_APD1 : process (sysclk,COUNT_SIG1,sync_out1)
242     begin
243 if (COUNT_SIG1 = '1') then
244 --      if (COUNT_SIGNAL(1) = '0') then
245             pulse_out1 <= '1';
246         elsif (sync_out1 = '1') then
247             pulse_out1 <= '0';
248         elsif (SYSCLK'event and SYSCLK ='1') then
249             if (sync_out1 = '1') then
250                 pulse_out1 <= '0';
251             end if;
252         end if;
253     end process;
254
255     sync1 : process (SYSCLK,pulse_out1)
256     begin
257         if (SYSCLK'event and SYSCLK ='1') then
258             sync_out1 <= pulse_out1;
259         end if;
260     end process;
261
262
263 --  pulse_APD2 : process (SYSCLK,COUNT_SIGNAL(2),sync_out2)
264 pulse_APD2 : process (SYSCLK,COUNT_SIG2,sync_out2)
265 begin
266 if (COUNT_SIG2 = '1') then
267 --  if (COUNT_SIGNAL(2) = '0') then
268             pulse_out2 <= '1';
269         elsif (sync_out2 = '1') then
270             pulse_out2 <= '0';
271         elsif (SYSCLK'event and SYSCLK ='1') then
272             if (sync_out2 = '1') then
273                 pulse_out2 <= '0';
274             end if;
275         end if;
276     end process;
277
278     sync2 : process (SYSCLK,pulse_out2)
279     begin
280         if (SYSCLK'event and SYSCLK ='1') then
281             sync_out2 <= pulse_out2;
282         end if;
283     end process;
284
285
286 --  pulse_APD3 : process (SYSCLK,COUNT_SIGNAL(3),sync_out3)
287 pulse_APD3 : process (SYSCLK,COUNT_SIG3,sync_out3)
288 begin
289 if (COUNT_SIG3 = '1') then
290 --  if (COUNT_SIGNAL(3) = '0') then
291             pulse_out3 <= '1';
292         elsif (sync_out3 = '1') then
```

```
293             pulse_out3 <= '0';
294         elsif (SYSCLK'event and SYSCLK ='1') then
295             if (sync_out3 = '1') then
296                 pulse_out3 <= '0';
297             end if;
298         end if;
299     end process;
300
301     sync3 : process (SYSCLK,pulse_out3)
302     begin
303         if (SYSCLK'event and SYSCLK ='1') then
304             sync_out3 <= pulse_out3;
305         end if;
306     end process;
307
308
309 --  pulse_APD4 : process (SYSCLK,COUNT_SIGNAL(4),sync_out4)
310     pulse_APD4 : process (SYSCLK,COUNT_SIG4,sync_out4)
311     begin
312 if (COUNT_SIG4 = '1') then
313 --  if (COUNT_SIGNAL(4) = '0') then
314             pulse_out4 <= '1';
315         elsif (sync_out4 = '1') then
316             pulse_out4 <= '0';
317         elsif (SYSCLK'event and SYSCLK ='1') then
318             if (sync_out4 = '1') then
319                 pulse_out4 <= '0';
320             end if;
321         end if;
322     end process;
323
324     sync4 : process (SYSCLK,pulse_out4)
325     begin
326         if (SYSCLK'event and SYSCLK ='1') then
327             sync_out4 <= pulse_out4;
328         end if;
329     end process;
330
331     -- Register TempCount to make it fit
332     reg_count : process (SYSCLK)
333     begin
334         if (SYSCLK'event and SYSCLK ='1') then
335             TempCount1 <= TempCount;
336         end if;
337     end process;
338
339     -- If C[5:1] matches DCI[2:0] and Output_En = '1' drive outputs
340     -- else set outputs to HighZ
341 --  D(13 downto 0)  <= TempCount1(13 downto 0) when (DCI(2 downto 0) = C(5 downto 3)) else (others
342 --  D(15 downto 14) <= "00" when (DCI(2 downto 0) = C(5 downto 3)) else (others => 'Z');
343 D(14 downto 0)  <= TempCount1(14 downto 0) when (DCI(2 downto 0) = C(5 downto 3)) else (others =>
344 D(15) <= '0' when (DCI(2 downto 0) = C(5 downto 3)) else ('Z');
345
346 OUTEN <= sync_out2;
347 -- debug
348 --  OUTEN <= '1' when (DCI(2 downto 0) = C(5 downto 3)) else '0';
349 -- end debug
350 end Counter;
```

```
 1 --
 2 --  This is a 16-bit asynchronous counter w/ count enable and reset
 3 --
 4 --  ***************************************************************
 5 --  Revision history
 6 --
 7 --  Date        Rev Eng             Description
 8 --  --------    --- --------------  ---------------------
 9 --  12/16/02    1   RY              Initial File
10 --  1/3/03      2   PMO             change counter 13bit to fit
11 --  1/6/03      3   PMO             sync counter
12
13 library IEEE;
14 use IEEE.std_logic_1164.all;
15 use IEEE.std_logic_unsigned.all;
16
17 entity sync_Counter is
18     port (
19         RESET:      in STD_LOGIC;
20         COUNT_EN:   in STD_LOGIC;
21         D_IN:   in STD_LOGIC;
22         clk:    in STD_LOGIC;
23 --      COUNT_OUT:  out STD_LOGIC_VECTOR(13 downto 0)
24         COUNT_OUT:  out STD_LOGIC_VECTOR(14 downto 0)
25         );
26 end sync_Counter;
27
28 architecture sync_Counter of sync_Counter is
29 --   signal TempCount:  STD_LOGIC_VECTOR(13 downto 0);
30 -- signal TempCount:    STD_LOGIC_VECTOR(11 downto 0);
31 begin
32     count : process (clk,D_IN, COUNT_EN, RESET)
33     begin
34         if ((RESET = '1')) then
35         COUNT_OUT   <= (others => '0');
36 --      TempCount   <= (others => '0');
37         elsif (clk'event and clk = '1') then
38 --      elsif (D_IN'event and D_IN = '1') then
39             if (COUNT_EN = '1' and D_IN = '1') then
40 --              TempCount   <= TempCount + 1;
41                 COUNT_OUT   <=  COUNT_OUT +1;
42             end if;
43         end if;
44     end process;
45
46 --  COUNT_OUT <= TempCount;
47 end sync_Counter;
```

```
Attribute PIN_NUMBERS of DCO(0)             is      "2";
Attribute PIN_NUMBERS of DCO(1)             is      "3";
Attribute PIN_NUMBERS of DCO(2)             is      "4";
Attribute PIN_NUMBERS of DCO(3)             is      "5";
Attribute PIN_NUMBERS of DCO(4)             is      "7";
Attribute PIN_NUMBERS of DCO(5)             is      "8";
Attribute PIN_NUMBERS of DCO(6)             is      "9";
Attribute PIN_NUMBERS of DCO(7)             is      "11";
Attribute PIN_NUMBERS of DCO(8)             is      "12";
Attribute PIN_NUMBERS of DCO(9)             is      "13";
Attribute PIN_NUMBERS of DCO(10)            is      "14";
Attribute PIN_NUMBERS of DCO(11)            is      "15";
Attribute PIN_NUMBERS of DCO(12)            is      "16";
Attribute PIN_NUMBERS of DCO(13)            is      "17";
Attribute PIN_NUMBERS of DCO(14)            is      "18";

Attribute PIN_NUMBERS of SYSCLK             is      "19";
Attribute PIN_NUMBERS of COUNT_SIGNAL(1)    is  "23";
Attribute PIN_NUMBERS of COUNT_SIGNAL(2)    is  "24";

Attribute PIN_NUMBERS of OUTEN          is  "42";
-- Attribute PIN_NUMBERS of RESET_CNT       is  "78";

Attribute PIN_NUMBERS of DCI(0)         is  "119";
Attribute PIN_NUMBERS of DCI(1)         is  "118";
Attribute PIN_NUMBERS of DCI(2)         is  "117";
Attribute PIN_NUMBERS of DCI(3)         is  "115";
Attribute PIN_NUMBERS of DCI(4)         is  "114";
Attribute PIN_NUMBERS of DCI(5)         is  "113";
Attribute PIN_NUMBERS of DCI(6)         is  "112";
Attribute PIN_NUMBERS of DCI(7)         is  "110";
Attribute PIN_NUMBERS of DCI(8)         is  "109";
Attribute PIN_NUMBERS of DCI(9)         is  "108";
Attribute PIN_NUMBERS of DCI(10)            is  "107";
Attribute PIN_NUMBERS of DCI(11)            is  "106";
Attribute PIN_NUMBERS of DCI(12)            is  "105";
Attribute PIN_NUMBERS of DCI(13)            is  "104";
Attribute PIN_NUMBERS of DCI(14)            is  "103";

Attribute PIN_NUMBERS of COUNT_SIGNAL(4)    is  "98";
Attribute PIN_NUMBERS of COUNT_SIGNAL(3)    is  "97";

Attribute PIN_NUMBERS of D(0)           is  "138";
Attribute PIN_NUMBERS of D(1)           is  "137";
Attribute PIN_NUMBERS of D(2)           is  "136";
Attribute PIN_NUMBERS of D(3)           is  "135";
Attribute PIN_NUMBERS of D(4)           is  "134";
Attribute PIN_NUMBERS of D(5)           is  "133";
Attribute PIN_NUMBERS of D(6)           is  "132";
Attribute PIN_NUMBERS of D(7)           is  "131";
Attribute PIN_NUMBERS of D(8)           is  "129";
Attribute PIN_NUMBERS of D(9)           is  "128";
Attribute PIN_NUMBERS of D(10)          is  "127";
Attribute PIN_NUMBERS of D(11)          is  "126";
Attribute PIN_NUMBERS of D(12)          is  "125";
Attribute PIN_NUMBERS of D(13)          is  "124";
Attribute PIN_NUMBERS of D(14)          is  "123";
Attribute PIN_NUMBERS of D(15)          is  "122";

Attribute PIN_NUMBERS of C(0)           is  "159";
Attribute PIN_NUMBERS of C(1)           is  "158";
Attribute PIN_NUMBERS of C(2)           is  "157";
Attribute PIN_NUMBERS of C(3)           is  "156";
Attribute PIN_NUMBERS of C(4)           is  "155";
Attribute PIN_NUMBERS of C(5)           is  "154";
Attribute PIN_NUMBERS of C(6)           is  "153";
Attribute PIN_NUMBERS of C(7)           is  "152";
Attribute PIN_NUMBERS of C(8)           is  "150";
Attribute PIN_NUMBERS of C(9)           is  "149";
Attribute PIN_NUMBERS of C(10)          is  "148";
Attribute PIN_NUMBERS of C(11)          is  "147";
Attribute PIN_NUMBERS of C(12)          is  "146";
Attribute PIN_NUMBERS of C(13)          is  "145";
```

```
74 Attribute PIN_NUMBERS of C(14)          is  "144";
75 Attribute PIN_NUMBERS of C(15)          is  "143";
76
77 --DEBUG
78 --Attribute PIN_NUMBERS of OUTEN           is  "48";
79 --END DEBUG
```

4.3 Test Control Chip

```
 1 --
 2 --  Pulse Generator
 3 --  This is a test chip for the Counter boards.  It creates 1 pulse
 4 --  every X clock pulses.  Where X is the value that read from the
 5 --  C[7:0].  Note:  value is a binary value
 6 --
 7 --  ************************************************************
 8 --  Revision history
 9 --
10 --  Date        Rev Eng             Description
11 --  --------    --- --------------  ----------------------
12 --  01/13/02    1   RY              Initial File
13 --
14
15 library IEEE;
16 use IEEE.std_logic_1164.all;
17 use IEEE.std_logic_unsigned.all;
18
19 entity PulseGenControl is
20     port(
21         LED :               out std_logic_vector(3 downto 1);
22         SYSCLK:             in STD_LOGIC;
23         --
24         -- backplane data bus and associated control signal
25         --
26 --      BPADDR:             in std_logic_vector(7 downto 0);
27         BPCTRL:             in std_logic_vector(8 downto 0);
28 --      BPCTRL:             in std_logic_vector(15 downto 0);
29 --      BPD:                out std_logic_vector(15 downto 0);
30         BPD_L_TRISTATE:     out std_logic;
31         BPD_H_TRISTATE:     out std_logic;
32         bpd_h_dir:          out std_logic;
33         bpd_l_dir:          out std_logic;
34         bpaddr_dir:         out std_logic;
35         bpaddr_tristate:    out std_logic;
36         bpctrl_h_dir:       out std_logic;
37         bpctrl_l_dir:       out std_logic;
38         bpctrl_h_tristate:  out std_logic;
39         bpctrl_l_tristate:  out std_logic;
40         SW:                 in std_logic_vector(7 downto 0);
41         --
42         -- internal bus
43         --
44 --      D:                  in std_logic_vector(15 downto 0);
45         C:                  out std_logic_vector(15 downto 0)
46     );
47 end PulseGenControl;
48
49 architecture PulseGenControl of PulseGenControl is
50 begin
51     -- constant signals
52     C(15 downto 9)  <= (others => 'Z');
53     bpd_h_dir <= '0';
54     bpd_l_dir <= '0';
55     bpaddr_dir <= '1';
56     bpaddr_tristate <= '0';
57     bpctrl_h_dir <= '0';
58     bpctrl_l_dir <= '1';
59     bpctrl_h_tristate <= '1';
60     bpctrl_l_tristate <= '0';
61     BPD_L_TRISTATE <=  '1';
62     BPD_H_TRISTATE <= '1';
63     LED(3 downto 2) <= "00";
64
65     Control : process(SYSCLK, BPCTRL(1), SW)
66     begin
67         if (SYSCLK'event and SYSCLK = '1') then
68             C(0)            <= BPCTRL(1);
69             C(8 downto 1)   <= SW;
70             LED(1)          <= BPCTRL(1);
71         end if;
72     end process;
73
```

```
74
75 end PulseGenControl;
```

```
---
-- Digital to analog converter control lines
--
--
-- Bus Address control
--
Attribute PIN_NUMBERS of bpctrl_h_tristate is   "3";
Attribute PIN_NUMBERS of bpd_l_tristate is  "4";
Attribute PIN_NUMBERS of bpctrl_l_dir is    "5";
--
-- Bus Data control
--
Attribute PIN_NUMBERS of bpctrl_l_tristate is   "7";
Attribute PIN_NUMBERS of bpctrl_h_dir is    "8";
Attribute PIN_NUMBERS of bpd_l_dir is       "9";
--
-- Bus Ctrl signals
Attribute PIN_NUMBERS of bpctrl(0) is       "11";
Attribute PIN_NUMBERS of bpctrl(1) is       "12";
Attribute PIN_NUMBERS of bpctrl(2) is       "13";
Attribute PIN_NUMBERS of bpctrl(3) is       "14";
Attribute PIN_NUMBERS of bpctrl(4) is       "15";
Attribute PIN_NUMBERS of bpctrl(5) is       "16";
Attribute PIN_NUMBERS of bpctrl(6) is       "17";
Attribute PIN_NUMBERS of bpctrl(7) is       "18";
Attribute PIN_NUMBERS of bpctrl(8) is       "23";
Attribute PIN_NUMBERS of bpctrl(9) is       "24";
Attribute PIN_NUMBERS of bpctrl(10) is      "25";
Attribute PIN_NUMBERS of bpctrl(11) is      "26";
Attribute PIN_NUMBERS of bpctrl(12) is      "27";
Attribute PIN_NUMBERS of bpctrl(13) is      "28";
Attribute PIN_NUMBERS of bpctrl(14) is      "29";
Attribute PIN_NUMBERS of bpctrl(15) is      "30";
--
-- Power up pins attached to r/c timers
--
Attribute PIN_NUMBERS of SYSCLK is          "19";
--
-- Bus address signals
--
Attribute PIN_NUMBERS of bpaddr(0) is       "32";
Attribute PIN_NUMBERS of bpaddr(1) is       "33";
Attribute PIN_NUMBERS of bpaddr(2) is       "34";
Attribute PIN_NUMBERS of bpaddr(3) is       "35";
Attribute PIN_NUMBERS of bpaddr(4) is       "36";
Attribute PIN_NUMBERS of bpaddr(5) is       "37";
Attribute PIN_NUMBERS of bpaddr(6) is       "38";
Attribute PIN_NUMBERS of bpaddr(7) is       "39";

--
-- Bus control control
--
Attribute PIN_NUMBERS of bpd_h_dir is       "43";
Attribute PIN_NUMBERS of bpd_h_tristate is  "42";
Attribute PIN_NUMBERS of bpaddr_tristate is "44";
Attribute PIN_NUMBERS of bpaddr_dir is      "45";
--
-- Lines driving LED's
--
Attribute PIN_NUMBERS of led(1) is    "47";
Attribute PIN_NUMBERS of led(2) is        "48";
Attribute PIN_NUMBERS of led(3) is        "49";
--
-- Address switch lines
--
Attribute PIN_NUMBERS of sw(3) is        "51";
Attribute PIN_NUMBERS of sw(2) is        "52";
Attribute PIN_NUMBERS of sw(1) is        "53";
Attribute PIN_NUMBERS of sw(0) is        "54";
Attribute PIN_NUMBERS of sw(7) is        "55";
Attribute PIN_NUMBERS of sw(6) is        "56";
Attribute PIN_NUMBERS of sw(5) is        "57";
Attribute PIN_NUMBERS of sw(4) is        "58";

Attribute PIN_NUMBERS of RESET_CNT is       "78";
```

```
 76
 77 Attribute PIN_NUMBERS of c(0) is    "98"; -- Not available on 192 version.
 78 Attribute PIN_NUMBERS of c(1) is    "103";
 79 Attribute PIN_NUMBERS of c(2) is    "104";
 80 Attribute PIN_NUMBERS of c(3) is    "105";
 81 Attribute PIN_NUMBERS of c(4) is    "106";
 82 Attribute PIN_NUMBERS of c(5) is    "107";
 83 Attribute PIN_NUMBERS of c(6) is    "108";
 84 Attribute PIN_NUMBERS of c(7) is    "109";
 85 Attribute PIN_NUMBERS of c(8) is    "110";
 86 Attribute PIN_NUMBERS of c(9) is    "112";
 87 Attribute PIN_NUMBERS of c(10) is   "113";
 88 Attribute PIN_NUMBERS of c(11) is   "114";
 89 Attribute PIN_NUMBERS of c(12) is   "115";
 90 Attribute PIN_NUMBERS of c(13) is   "117";
 91 Attribute PIN_NUMBERS of c(14) is   "118";
 92 Attribute PIN_NUMBERS of c(15) is   "119";
 93
 94 Attribute PIN_NUMBERS of d(15) is   "122"; -- Not available on 192 version.
 95 Attribute PIN_NUMBERS of d(14) is   "123";
 96 Attribute PIN_NUMBERS of d(13) is   "124";
 97 Attribute PIN_NUMBERS of d(12) is   "125";
 98 Attribute PIN_NUMBERS of d(11) is   "126";
 99 Attribute PIN_NUMBERS of d(10) is   "127";
100 Attribute PIN_NUMBERS of d(9) is    "128";
101 Attribute PIN_NUMBERS of d(8) is    "129";
102 Attribute PIN_NUMBERS of d(7) is    "131";
103 Attribute PIN_NUMBERS of d(6) is    "132";
104 Attribute PIN_NUMBERS of d(5) is    "133";
105 Attribute PIN_NUMBERS of d(4) is    "134";
106 Attribute PIN_NUMBERS of d(3) is    "135";
107 Attribute PIN_NUMBERS of d(2) is    "136";
108 Attribute PIN_NUMBERS of d(1) is    "137";
109 Attribute PIN_NUMBERS of d(0) is    "138";
110
111 --
112 -- Bus data signals
113 --
114 Attribute PIN_NUMBERS of bpd(0) is  "143";
115 Attribute PIN_NUMBERS of bpd(1) is  "144";
116 Attribute PIN_NUMBERS of bpd(2) is  "145";
117 Attribute PIN_NUMBERS of bpd(3) is  "146";
118 Attribute PIN_NUMBERS of bpd(4) is  "147";
119 Attribute PIN_NUMBERS of bpd(5) is  "148";
120 Attribute PIN_NUMBERS of bpd(6) is  "149";
121 Attribute PIN_NUMBERS of bpd(7) is  "150";
122 Attribute PIN_NUMBERS of bpd(8) is  "152";
123 Attribute PIN_NUMBERS of bpd(9) is  "153";
124 Attribute PIN_NUMBERS of bpd(10) is "154";
125 Attribute PIN_NUMBERS of bpd(11) is "155";
126 Attribute PIN_NUMBERS of bpd(12) is "156";
127 Attribute PIN_NUMBERS of bpd(13) is "157";
128 Attribute PIN_NUMBERS of bpd(14) is "158";
129 Attribute PIN_NUMBERS of bpd(15) is "159";
130
131
132
133
134
```

4.4 Test Counter Chip

```
--
--  Pulse Generator
--  This is a test chip for the Counter boards.  It creates 1 pulse
--  every X clock pulses.  Where X is the value that read from the
--  C[7:0].  Note:  value is a binary value
--
--  ************************************************************
--  Revision history
--
--  Date        Rev Eng             Description
--  --------    --- --------------  ----------------------
--  12/16/02    1   RY              Initial File
--

library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity PulseGen is
    port (
        SYSCLK:         in STD_LOGIC;
        C:              in STD_LOGIC_VECTOR(8 downto 0);
        PULSE_OUT:      out STD_LOGIC_VECTOR(4 downto 1);
        D:              out STD_LOGIC_VECTOR(15 downto 0);
        DCI:            in STD_LOGIC_VECTOR(14 downto 0);
        DCO:            out STD_LOGIC_VECTOR(14 downto 0)
        );
end PulseGen;

architecture PulseGen of PulseGen is
    signal count:       STD_LOGIC_VECTOR(15 downto 0):=(others => '0');
    signal pulse:       STD_LOGIC;
    signal max_count:   STD_LOGIC_VECTOR(15 downto 0);
begin
    MaxCount : process (SYSCLK, C(5 downto 1))
    begin
        if (SYSCLK'event and SYSCLK = '1') then
            -- NOTE: C(5 downto 1) coresponds to SW(5 downto 1)
            case (C(5 downto 1)) is
                when "00000" => max_count <= x"0002";
                when "00001" => max_count <= x"0004";
                when "00010" => max_count <= x"0008";
                when "00011" => max_count <= x"0010";
                when "00100" => max_count <= x"0020";
                when "00101" => max_count <= x"0040";
                when "00110" => max_count <= x"0080";
                when "00111" => max_count <= x"0100";
                when "01000" => max_count <= x"0200";
                when "01001" => max_count <= x"0400";
                when "01010" => max_count <= x"0800";
                when "01011" => max_count <= x"1000";
                when "01100" => max_count <= x"2000";
                when "01101" => max_count <= x"4000";
                when "01110" => max_count <= x"8000";
                when "01111" => max_count <= x"FFFF";
                when others => max_count <= x"0003";
            end case;
        end if;
    end process;

    -- Count until counter hits value on C then create pulse and reset counter
    Counter : process (SYSCLK, C)
    begin
        if (SYSCLK'event and SYSCLK = '1') then
            if (count = max_count)then
                pulse <= '1';
                count <= (others => '0');
                -- write value of count to DCO for debugging
                DCO(13 downto 0) <= count(13 downto 0);
        else
                pulse <= '0';
                count <= count + 1;
                -- write value of count to DCO for debugging
```

```
                DCO(13 downto 0) <= count(13 downto 0);
            end if;
        end if;
    end process;

    -- for debugging, route clock signal to DCO(14)
    DCO(14) <= SYSCLK;

    Output : process (SYSCLK, C(8 downto 6))
    begin
        if (SYSCLK'event and SYSCLK = '1') then
            -- NOTE: C(58 downto 6) coresponds to SW(8 downto 6)
            case (C(8 downto 6)) is
                -- No Counts - All zeros
                when "000" =>
                    PULSE_OUT(1) <= '0';
                    PULSE_OUT(2) <= '0';
                    PULSE_OUT(3) <= '0';
                    PULSE_OUT(4) <= '0';
                -- Low Counts ONLY
                when "001" =>
                    if (C(0)='0') then
                        PULSE_OUT(1) <= pulse;
                        PULSE_OUT(2) <= pulse;
                        PULSE_OUT(3) <= pulse;
                        PULSE_OUT(4) <= pulse;
                    else
                        PULSE_OUT(1) <= '0';
                        PULSE_OUT(2) <= '0';
                        PULSE_OUT(3) <= '0';
                        PULSE_OUT(4) <= '0';
                    end if;
                -- High Counts ONLY
                when "010" =>
                    if (C(0)='1') then
                        PULSE_OUT(1) <= pulse;
                        PULSE_OUT(2) <= pulse;
                        PULSE_OUT(3) <= pulse;
                        PULSE_OUT(4) <= pulse;
                    else
                        PULSE_OUT(1) <= '0';
                        PULSE_OUT(2) <= '0';
                        PULSE_OUT(3) <= '0';
                        PULSE_OUT(4) <= '0';
                    end if;
                -- Count ALL
                when "011" =>
                    PULSE_OUT(1) <= pulse;
                    PULSE_OUT(2) <= pulse;
                    PULSE_OUT(3) <= pulse;
                    PULSE_OUT(4) <= pulse;
                when others =>
                    PULSE_OUT(1) <= pulse;
                    PULSE_OUT(2) <= pulse;
                    PULSE_OUT(3) <= pulse;
                    PULSE_OUT(4) <= pulse;
            end case;
        end if;
    end process;
end PulseGen;
```

```
 1 Attribute PIN_NUMBERS of DCO(0)            is      "2";
 2 Attribute PIN_NUMBERS of DCO(1)            is      "3";
 3 Attribute PIN_NUMBERS of DCO(2)            is      "4";
 4 Attribute PIN_NUMBERS of DCO(3)            is      "5";
 5 Attribute PIN_NUMBERS of DCO(4)            is      "7";
 6 Attribute PIN_NUMBERS of DCO(5)            is      "8";
 7 Attribute PIN_NUMBERS of DCO(6)            is      "9";
 8 Attribute PIN_NUMBERS of DCO(7)            is      "11";
 9 Attribute PIN_NUMBERS of DCO(8)            is      "12";
10 Attribute PIN_NUMBERS of DCO(9)            is      "13";
11 Attribute PIN_NUMBERS of DCO(10)           is      "14";
12 Attribute PIN_NUMBERS of DCO(11)           is      "15";
13 Attribute PIN_NUMBERS of DCO(12)           is      "16";
14 Attribute PIN_NUMBERS of DCO(13)           is      "17";
15 Attribute PIN_NUMBERS of DCO(14)           is      "18";
16
17 Attribute PIN_NUMBERS of SYSCLK            is      "19";
18 Attribute PIN_NUMBERS of PULSE_OUT(1)   is  "23";
19 Attribute PIN_NUMBERS of PULSE_OUT(2)   is  "24";
20
21 -- Attribute PIN_NUMBERS of RESET_CNT       is  "78";
22
23 Attribute PIN_NUMBERS of DCI(0)         is  "119";
24 Attribute PIN_NUMBERS of DCI(1)         is  "118";
25 Attribute PIN_NUMBERS of DCI(2)         is  "117";
26 Attribute PIN_NUMBERS of DCI(3)         is  "115";
27 Attribute PIN_NUMBERS of DCI(4)         is  "114";
28 Attribute PIN_NUMBERS of DCI(5)         is  "113";
29 Attribute PIN_NUMBERS of DCI(6)         is  "112";
30 Attribute PIN_NUMBERS of DCI(7)         is  "110";
31 Attribute PIN_NUMBERS of DCI(8)         is  "109";
32 Attribute PIN_NUMBERS of DCI(9)         is  "108";
33 Attribute PIN_NUMBERS of DCI(10)            is  "107";
34 Attribute PIN_NUMBERS of DCI(11)            is  "106";
35 Attribute PIN_NUMBERS of DCI(12)            is  "105";
36 Attribute PIN_NUMBERS of DCI(13)            is  "104";
37 Attribute PIN_NUMBERS of DCI(14)            is  "103";
38
39 Attribute PIN_NUMBERS of PULSE_OUT(4)   is  "98";
40 Attribute PIN_NUMBERS of PULSE_OUT(3)   is  "97";
41
42 Attribute PIN_NUMBERS of D(0)           is  "138";
43 Attribute PIN_NUMBERS of D(1)           is  "137";
44 Attribute PIN_NUMBERS of D(2)           is  "136";
45 Attribute PIN_NUMBERS of D(3)           is  "135";
46 Attribute PIN_NUMBERS of D(4)           is  "134";
47 Attribute PIN_NUMBERS of D(5)           is  "133";
48 Attribute PIN_NUMBERS of D(6)           is  "132";
49 Attribute PIN_NUMBERS of D(7)           is  "131";
50 Attribute PIN_NUMBERS of D(8)           is  "129";
51 Attribute PIN_NUMBERS of D(9)           is  "128";
52 Attribute PIN_NUMBERS of D(10)          is  "127";
53 Attribute PIN_NUMBERS of D(11)          is  "126";
54 Attribute PIN_NUMBERS of D(12)          is  "125";
55 Attribute PIN_NUMBERS of D(13)          is  "124";
56 Attribute PIN_NUMBERS of D(14)          is  "123";
57 Attribute PIN_NUMBERS of D(15)          is  "122";
58
59 Attribute PIN_NUMBERS of C(0)           is  "159";
60 Attribute PIN_NUMBERS of C(1)           is  "158";
61 Attribute PIN_NUMBERS of C(2)           is  "157";
62 Attribute PIN_NUMBERS of C(3)           is  "156";
63 Attribute PIN_NUMBERS of C(4)           is  "155";
64 Attribute PIN_NUMBERS of C(5)           is  "154";
65 Attribute PIN_NUMBERS of C(6)           is  "153";
66 Attribute PIN_NUMBERS of C(7)           is  "152";
67 Attribute PIN_NUMBERS of C(8)           is  "150";
68 Attribute PIN_NUMBERS of C(9)           is  "149";
69 Attribute PIN_NUMBERS of C(10)          is  "148";
70 Attribute PIN_NUMBERS of C(11)          is  "147";
71 Attribute PIN_NUMBERS of C(12)          is  "146";
72 Attribute PIN_NUMBERS of C(13)          is  "145";
73 Attribute PIN_NUMBERS of C(14)          is  "144";
```

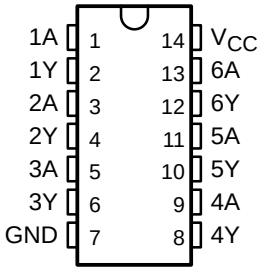
```
74 Attribute PIN_NUMBERS of C(15)          is  "143";
75
76 --DEBUG
77 --Attribute PIN_NUMBERS of OUTEN           is  "48";
78 --END DEBUG
```

5 Datasheets

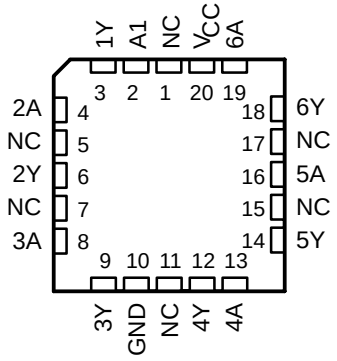
5.1 74AC14

- **2-V to 6-V V_{CC} Operation**
- **Inputs Accept Voltages to 6 V**
- **Max t_{pd} of 9.5 ns at 5 V**

SN54AC14 . . . J OR W PACKAGE
SN74AC14 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AC14 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These Schmitt-trigger devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$. Because of the Schmitt action, they have different input threshold levels for positive-going (V_{T+}) and for negative-going (V_{T-}) signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals. They also have a greater noise margin than conventional inverters.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AC14N	SN74AC14N
	SOIC – D	Tube	SN74AC14D	AC14
		Tape and reel	SN74AC14DR	
	SOP – NS	Tape and reel	SN74AC14NSR	AC14
	SSOP – DB	Tape and reel	SN74AC14DBR	AC14
	TSSOP – PW	Tape and reel	SN74AC14PWR	AC14
–55°C to 125°C	CDIP – J	Tube	SNJ54AC14J	SNJ54AC14J
	CFP – W	Tube	SNJ54AC14W	SNJ54AC14W
	LCCC – FK	Tube	SNJ54AC14FK	SNJ54AC14FK

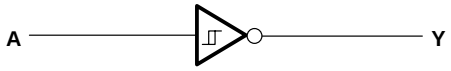
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

logic diagram, each inverter (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±200 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
PW package . . . . . 113°C/W
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54AC14		SN74AC14		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	6	2	6	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V		–12		–12	mA
		V_{CC} = 4.5 V		–24		–24	
		V_{CC} = 5.5 V		–24		–24	
I_{OL}	Low-level output current	V_{CC} = 3 V		12		12	mA
		V_{CC} = 4.5 V		24		24	
		V_{CC} = 5.5 V		24		24	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AC14		SN74AC14		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{T+} Positive-going threshold		3 V	0.8	1.8	2.2	0.8	2.2	0.8	2.2	V
		4.5 V	1.5	2.6	3.2	1.5	3.2	1.5	3.2	
		5.5 V	1.6	3.2	3.9	1.6	3.9	1.6	3.9	
V_{T-} Negative-going threshold		3 V	0.5	0.8	1	0.5	1	0.5	1	V
		4.5 V	0.9	1.4	1.8	0.9	1.8	0.9	1.8	
		5.5 V	1.1	1.8	2.3	1.1	2.3	1.1	2.3	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)		3 V	0.3	1	1.2	0.3	1.2	0.3	1.2	V
		4.5 V	0.4	1.2	1.4	0.4	1.4	0.4	1.4	
		5.5 V	0.5	1.4	1.6	0.5	1.6	0.5	1.6	
V_{OH}	I_{OH} = – 50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 12 mA	3 V	2.56			2.4		2.48		
	I_{OH} = – 24 mA	4.5 V	3.86			3.7		3.8		
		5.5 V	4.86			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 µA	3 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		5.5 V		0.001	0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			2		40		20	µA
C_i	$V_I = V_{CC}$ or GND	5 V		4.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			SN54AC14		SN74AC14		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	6	13.5	1	16	1.5	15	ns
t_{PHL}			1.5	6	11.5	1	14	1.5	13	

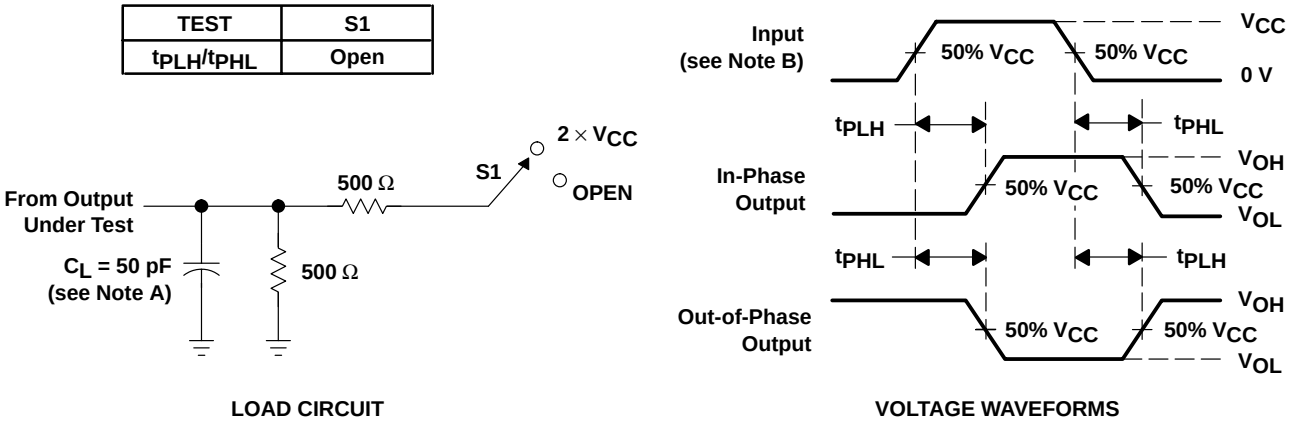
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			SN54AC14		SN74AC14		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	5	10	1.5	12	1.5	11	ns
t_{PHL}			1.5	5	8.5	1.5	10	1.5	9.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50pF,	f = 1 MHz	25	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

5.2 74ACT245

FAIRCHILD SEMICONDUCTOR™

November 1988
Revised November 1999

74AC245 • 74ACT245
Octal Bidirectional Transceiver with 3-STATE Inputs/Outputs

General Description

The AC/ACT245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 24 mA at both the A and B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

Features

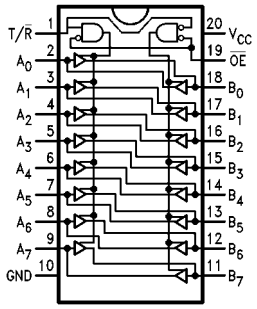
- I_{CC} and I_{OZ} reduced by 50%
- Noninverting buffers
- Bidirectional data path
- A and B outputs source/sink 24 mA
- ACT245 has TTL-compatible inputs

Ordering Code:

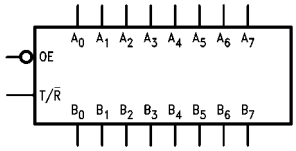
Order Number	Package Number	Package Description
74AC245SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300” Wide Body
74AC245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC245PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
74ACT245SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300” Wide Body
74ACT245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT245MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74ACT245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT245PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering code.

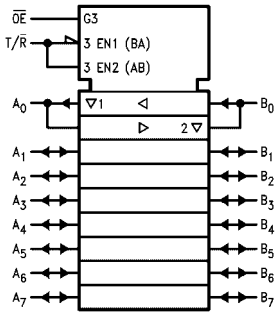
Connection Diagram



Logic Symbols



IEEE/IEC



Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A 3-STATE Inputs or 3-STATE Outputs
B_0–B_7	Side B 3-STATE Inputs or 3-STATE Outputs

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate (ΔV/Δt)	
AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt)	
ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	T_A = +25°C	T_A = −40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level	3.0	1.5	2.1	2.1		V_{OUT} = 0.1V
	Input Voltage	4.5	2.25	3.15	3.15	V	or V_{CC} − 0.1V
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum LOW Level	3.0	1.5	0.9	0.9		V_{OUT} = 0.1V
	Input Voltage	4.5	2.25	1.35	1.35	V	or V_{CC} − 0.1V
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum HIGH Level	3.0	2.99	2.9	2.9		
	Output Voltage	4.5	4.49	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4		
							V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.46		I_{OH} = −12 mA
		4.5		3.86	3.76	V	I_{OH} = −24 mA
		5.5		4.86	4.76		I_{OH} = −24 mA (Note 2)
V_{OL}	Maximum LOW Level	3.0	0.002	0.1	0.1		
	Output Voltage	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1		
							V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.44		I_{OL} = 12 mA
		4.5		0.36	0.44	V	I_{OL} = 24 mA
		5.5		0.36	0.44		I_{OL} = 24 mA (Note 2)
I_{IN} (Note 4)	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	V_I = V_{CC}, GND
I_{OLD}	Dynamic Output	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}	Current Minimum (Note 3)	5.5			−75	mA	V_{OHD} = 3.85V Min
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	V_{IN} = V_{CC} or GND
I_{OZT}	Maximum I/O						V_I (OE) = V_{IL}, V_{IH}
	Leakage Current	5.5		± 0.3	± 3.0	μA	V_I = V_{CC}, GND
							V_O = V_{CC}, GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

DC Characteristics for ACT

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Typ	$T_A = -40°C$ to $+85°C$ Guaranteed Limits		Units	Conditions
V_{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50\ \mu A$
		5.5	5.49	5.4	5.4		
		4.5		3.86	3.76	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24$ mA
		5.5		4.86	4.76		$I_{OH} = -24$ mA (Note 5)
V_{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		5.5	0.001	0.1	0.1		
		4.5		0.36	0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24$ mA
		5.5		0.36	0.44		$I_{OL} = 24$ mA (Note 5)
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	Dynamic Output Current Minimum (Note 6)	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}		5.5			−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.3	±3.0	μA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V) (Note 7)	$T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units
t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	3.3	1.5	5.0	8.5	1.0	9.0	ns
		5.0	1.5	3.5	6.5	1.0	7.0	
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	3.3	1.5	5.0	8.5	1.0	9.0	ns
		5.0	1.5	3.5	6.0	1.0	7.0	
t_{PZH}	Output Enable Time	3.3	2.5	7.0	11.5	2.0	12.5	ns
		5.0	1.5	5.0	8.5	1.0	9.0	
t_{PZL}	Output Enable Time	3.3	2.5	7.5	12.0	2.0	13.5	ns
		5.0	1.5	5.5	9.0	1.0	9.5	
t_{PHZ}	Output Disable Time	3.3	2.0	6.5	12.0	1.0	12.5	ns
		5.0	1.5	5.5	9.0	1.0	10.0	
t_{PLZ}	Output Disable Time	3.3	2.0	7.0	11.5	1.5	13.0	ns
		5.0	1.5	5.5	9.0	1.0	10.0	

Note 7: Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics for ACT

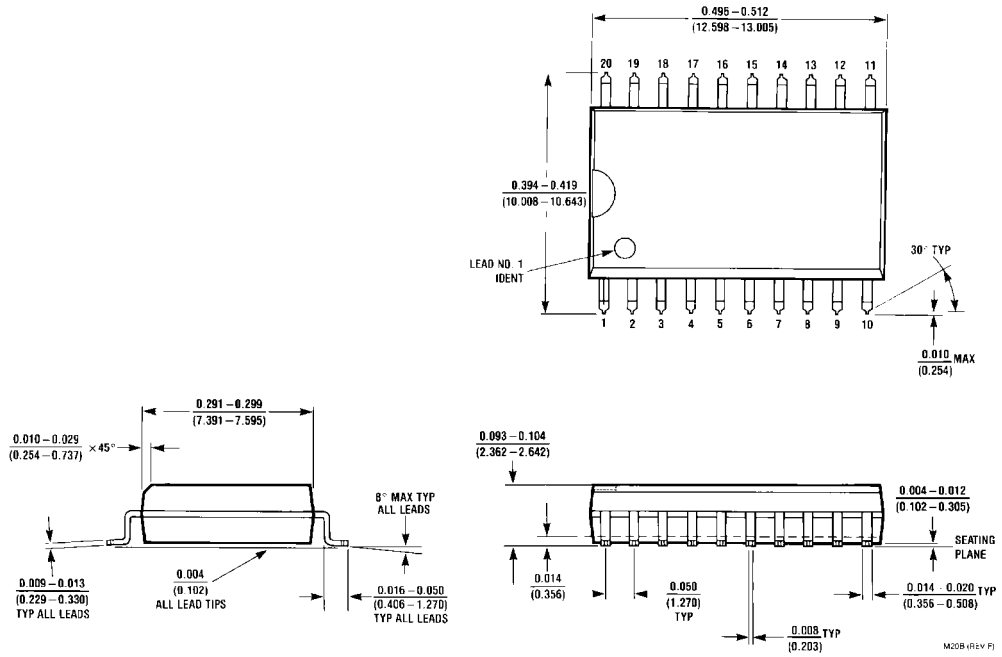
Symbol	Parameter	V_{CC} (V) (Note 8)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	5.0	1.5	4.0	7.5	1.5	8.0	ns
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	5.0	1.5	4.0	8.0	1.0	9.0	ns
t_{PZH}	Output Enable Time	5.0	1.5	5.0	10.0	1.5	11.0	ns
t_{PZL}	Output Enable Time	5.0	1.5	5.5	10.0	1.5	12.0	ns
t_{PHZ}	Output Disable Time	5.0	1.5	5.5	10.0	1.0	11.0	ns
t_{PLZ}	Output Disable Time	5.0	2.0	5.0	10.0	1.5	11.0	ns

Note 8: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

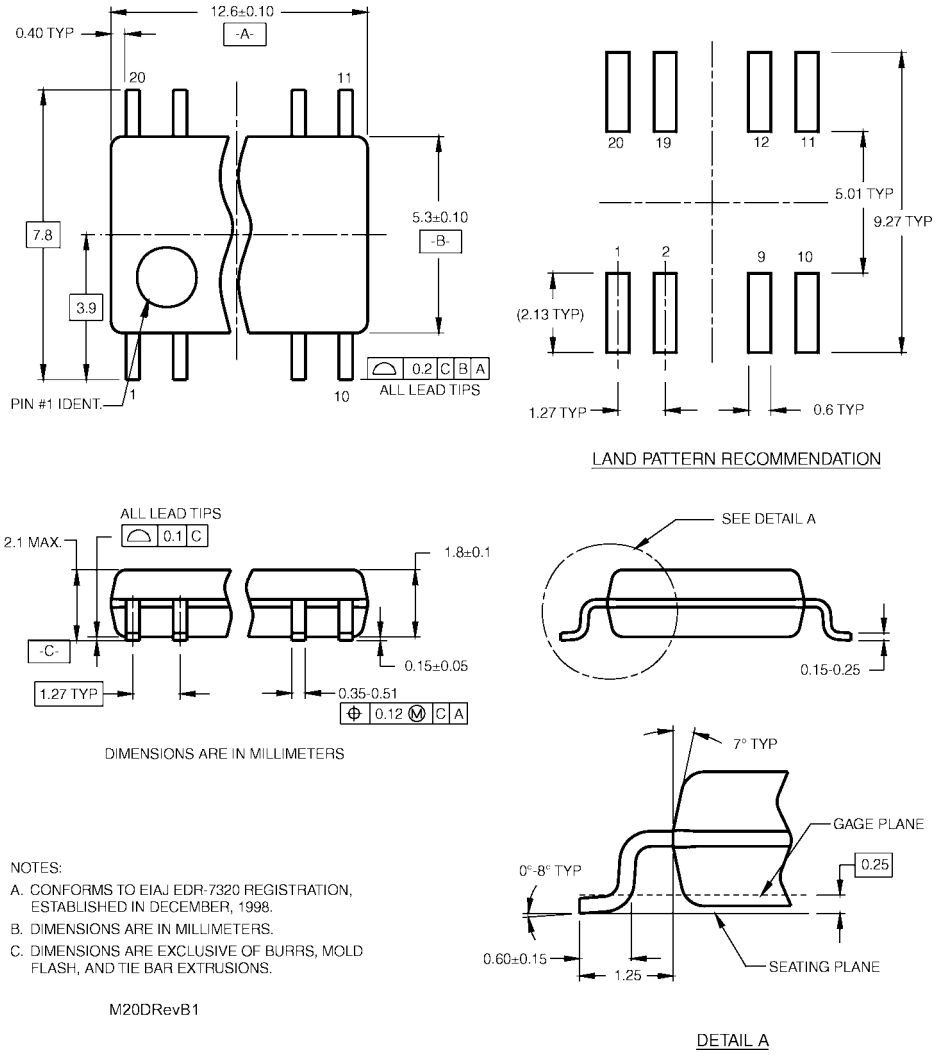
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
$C_{I/O}$	Input/Output Capacitance	15.0	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	45.0	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

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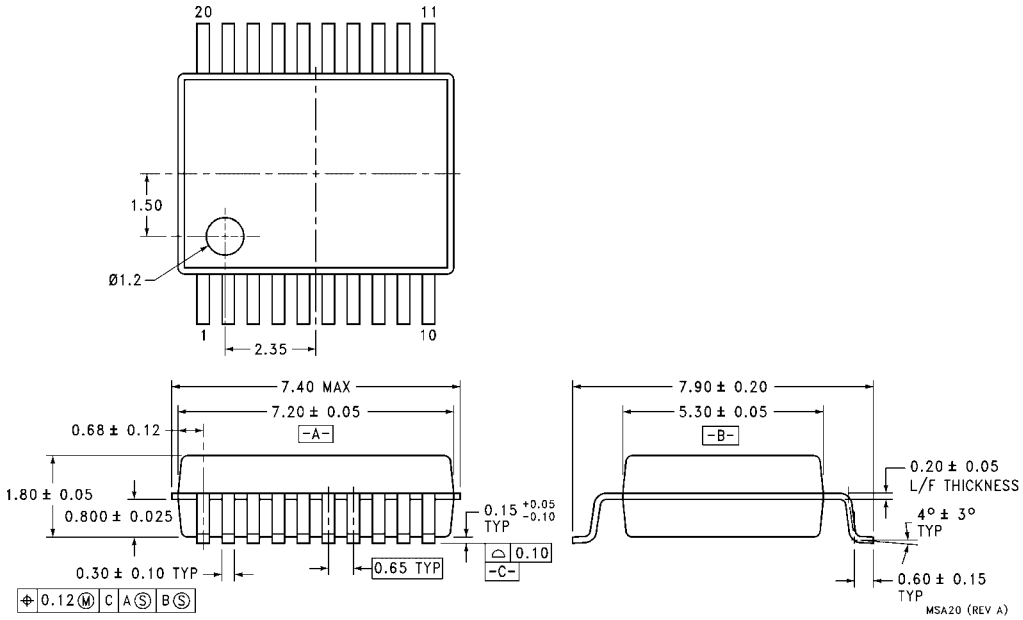
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

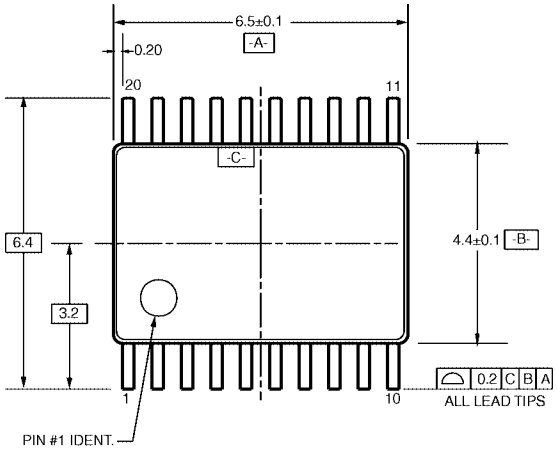
20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

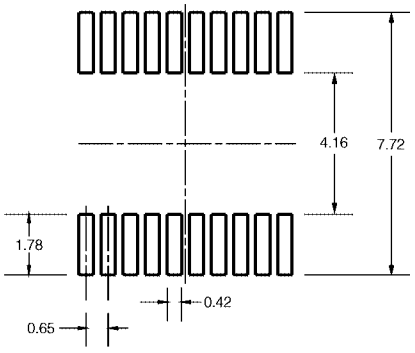
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



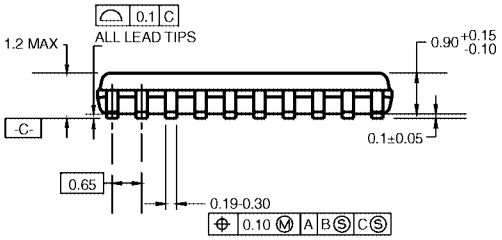
20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA20

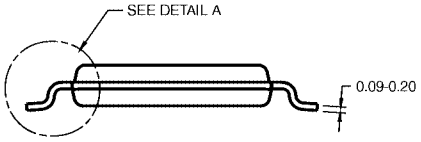
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)





LAND PATTERN RECOMMENDATION





DIMENSIONS ARE IN MILLIMETERS

NOTES:

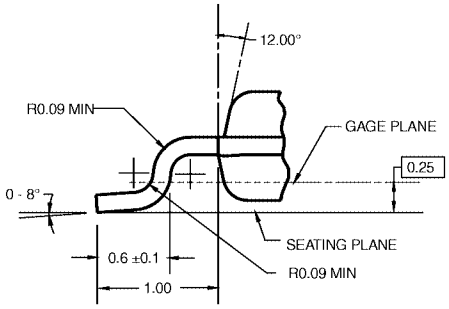
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

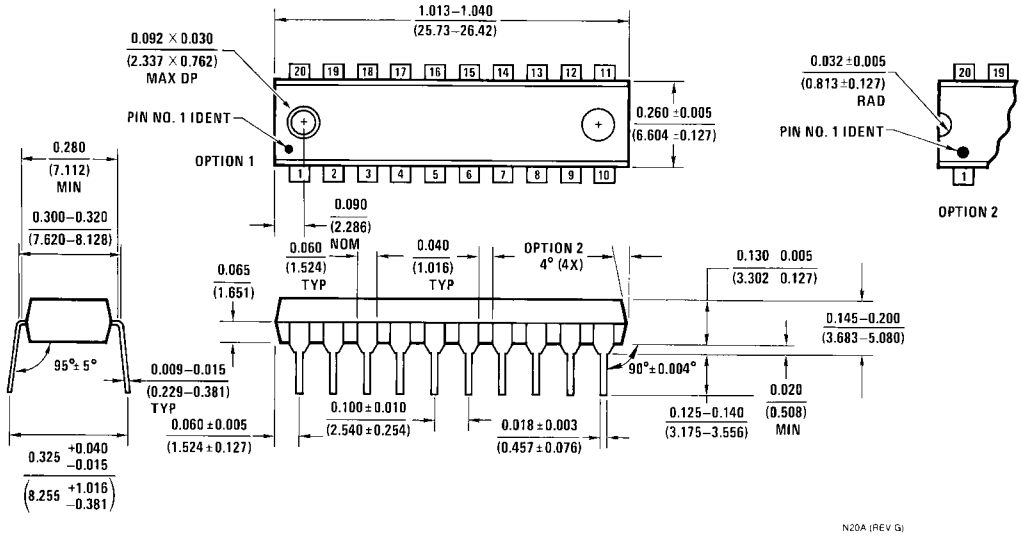
MTC20RevD1



DETAIL A

20-Lead Thin Shrink Small Outline Package, (TSSOP) JEDEC
Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

5.3 74HC132

CD54/74HC132, CD54/74HCT132

Data sheet acquired from Harris Semiconductor
SCHS145B

August 1997 - Revised December 2002

High Speed CMOS Logic Quad 2-Input NAND Schmitt Trigger

Features

- **Unlimited Input Rise and Fall Times**
- **Exceptionally High Noise Immunity**
- **Typical Propagation Delay: 10ns at V_{CC} = 5V, C_L = 15pF, T_A = 25^oC**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55^oC to 125^oC**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 37%, N_{IH} = 51% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The ’HC132 and ’HCT132 each contain four 2-input NAND Schmitt Triggers in one package. This logic device utilizes silicon gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The HCT logic family is functionally pin compatible with the standard LS logic family.

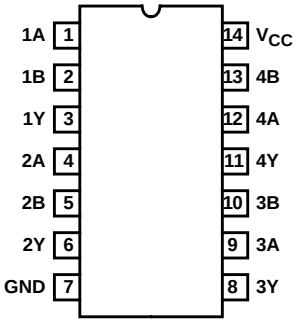
Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE
CD54HC132F3A	-55 to 125	14 Ld CERDIP
CD54HCT132F3A	-55 to 125	14 Ld CERDIP
CD74HC132E	-55 to 125	14 Ld PDIP
CD74HC132M	-55 to 125	14 Ld SOIC
CD74HC132M96	-55 to 125	14 Ld SOIC
CD74HCT132E	-55 to 125	14 Ld PDIP
CD74HCT132M	-55 to 125	14 Ld SOIC
CD74HCT132M96	-55 to 125	14 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel.

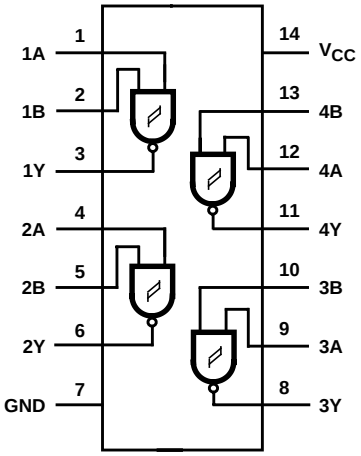
Pinout

CD54HC132, CD54HCT132
(CERDIP)
CD74HC132, CD74HCT132
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Functional Diagram

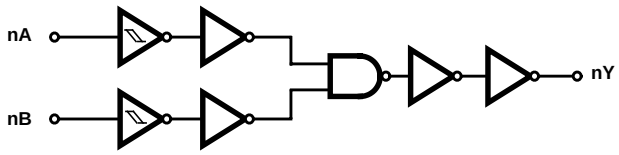


TRUTH TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

NOTE: H = High Voltage Level, L = Low Voltage Level

Logic Symbol



Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} or I_{GND} . . . . . ±50mA

Operating Conditions

Temperature Range (T_A) . . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . . 100ms (Max)
4.5V. . . . . 100ms (Max)
6V . . . . . 100ms (Max)

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
PDIP Package 80
SOIC Package 86
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
Input Switch Points (Note 2)	V_T+	-	-	2	0.7	-	1.5	0.7	1.5	0.7	1.5	V
				4.5	1.7	-	3.15	1.7	3.15	1.7	3.15	V
				6	2.1	-	4.2	2.1	4.2	2.1	4.2	V
	V_T-	-	-	2	0.3	-	1	0.3	1	0.3	1	V
				4.5	0.9	-	2.2	0.9	2.2	0.9	2.2	V
				6	1.2	-	3	1.2	3	1.2	3	V
	V_H			2	0.2	-	1	0.2	1	0.2	1	V
				4.5	0.4	-	1.4	0.4	1.4	0.4	1.4	V
				6	0.6	-	1.6	0.6	1.6	0.6	1.6	V
High Level Output Voltage CMOS Loads	V_{OH}	V_T+ or V_T-	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Low Level Output Voltage CMOS Loads	V_{OL}	V_T+ or V_T-	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	2	-	20	-	40	µA
HCT TYPES												
Input Switch Points (Note 2)	V_T+	-	-	4.5	1.2	-	1.9	1.2	1.9	1.2	1.9	V
				5.5	1.4	-	2.1	1.4	2.1	1.4	2.1	V
	V_T-	-	-	4.5	0.5	-	1.2	0.5	1.2	0.5	1.2	V
				5.5	0.6	-	1.4	0.6	1.4	0.6	1.4	V
	V_H	-	-	4.5	0.4	-	1.4	0.4	1.4	0.4	1.4	V
				5.5	0.4	-	1.5	0.4	1.5	0.4	1.5	V
High Level Output Voltage CMOS Loads	-	V_T+ or V_T-	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_T+ or V_T-	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} and GND	-	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	2	-	20	-	40	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 3)	ΔI_{CC}	V_{CC} - 2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTES:

2. Hysteresis definition, characteristic and test setup see Test Circuits and Waveforms
3. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
nA, nB	0.6

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g. 360µA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay A, B to Y (Figure 1)	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	125	-	156	-	188	ns
			4.5	-	-	25	-	31	-	38	ns
			6	-	-	21	-	27	-	32	ns
Propagation Delay A, B to Y	t_{TLH}, t_{THL}	C_L = 15pF	5	-	10	-	-	-	-	-	pF
Transition Times (Figure 1)	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	-	5	-	30	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay A, B to Y (Figure 2)	t_{PHL}, t_{PHL}	C_L = 50pF	4.5	-	-	33	-	41	-	50	ns
Propagation Delay A, B to Y	t_{PLH}, t_{PHL}	C_L = 15pF	5	-	13	-	-	-	-	-	pF
Transition Times (Figure 2)	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	-	5	-	30	-	-	-	-	-	pF

NOTES:

4. C_{PD} is used to determine the dynamic power consumption, per gate.
5. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

Test Circuits and Waveforms

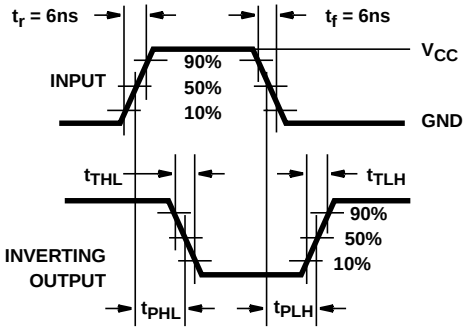


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

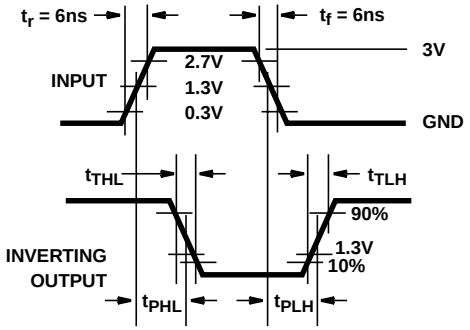


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

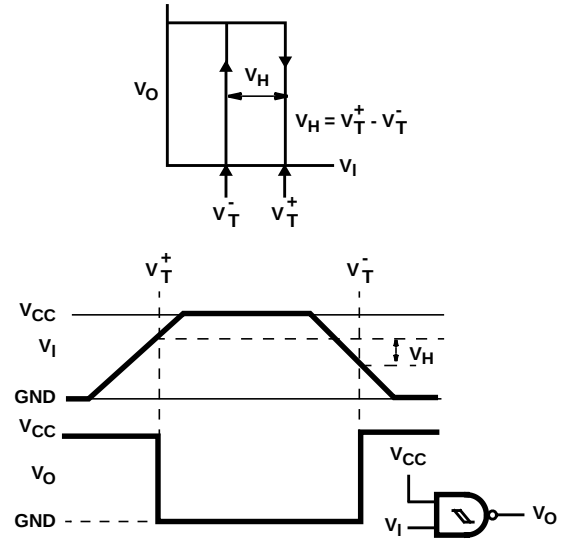
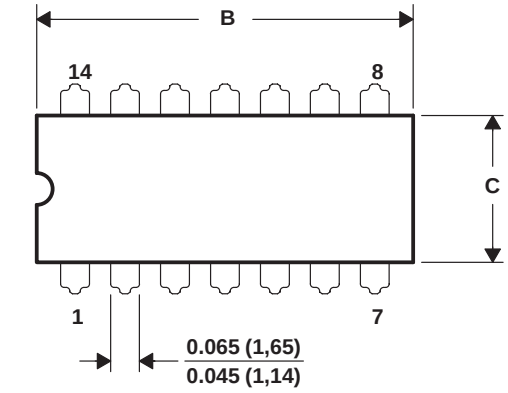


FIGURE 3. HYSTERESIS DEFINITION, CHARACTERISTIC, AND TEST SET-UP

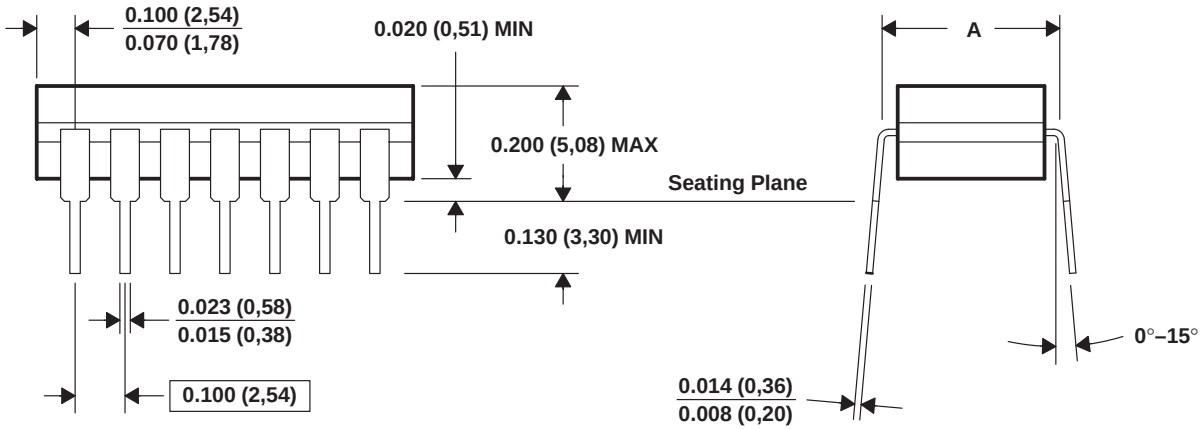
MCER002C – JANUARY 1995 – REVISED JUNE 1999

J (R-GDIP-T)** **CERAMIC DUAL-IN-LINE**

14 LEADS SHOWN



DIM \ PINS **	14	16	20
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)
B MAX	0.785 (19,94)	0.785 (19,94)	0.975 (24,77)
B MIN	0.755 (19,18)	0.755 (19,18)	0.930 (23,62)
C MAX	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)



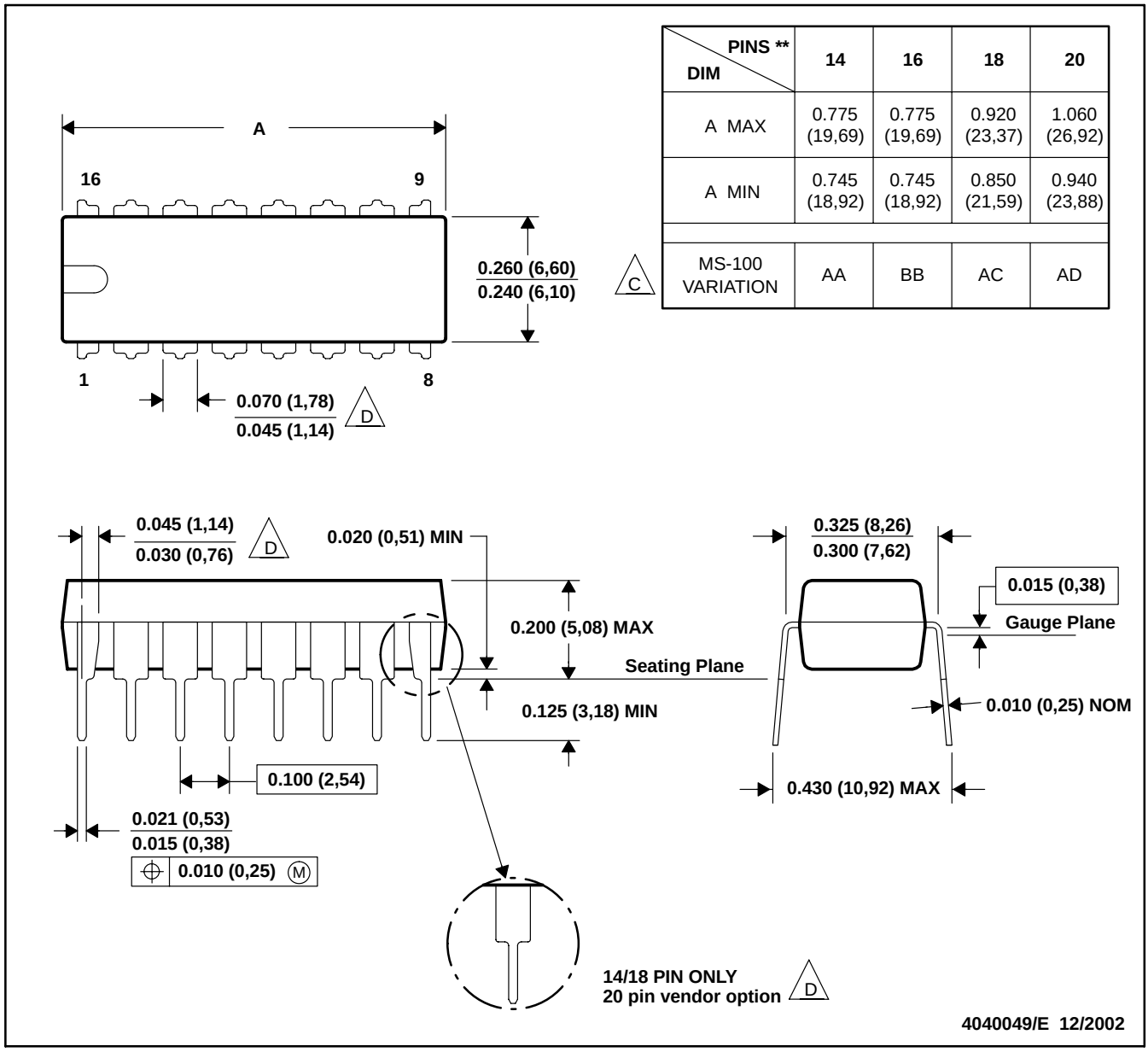
4040083/E 03/99

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, and GDIP1-T20

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-100 VARIATION	AA	BB	AC	AD

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body lrngth (Dim A).

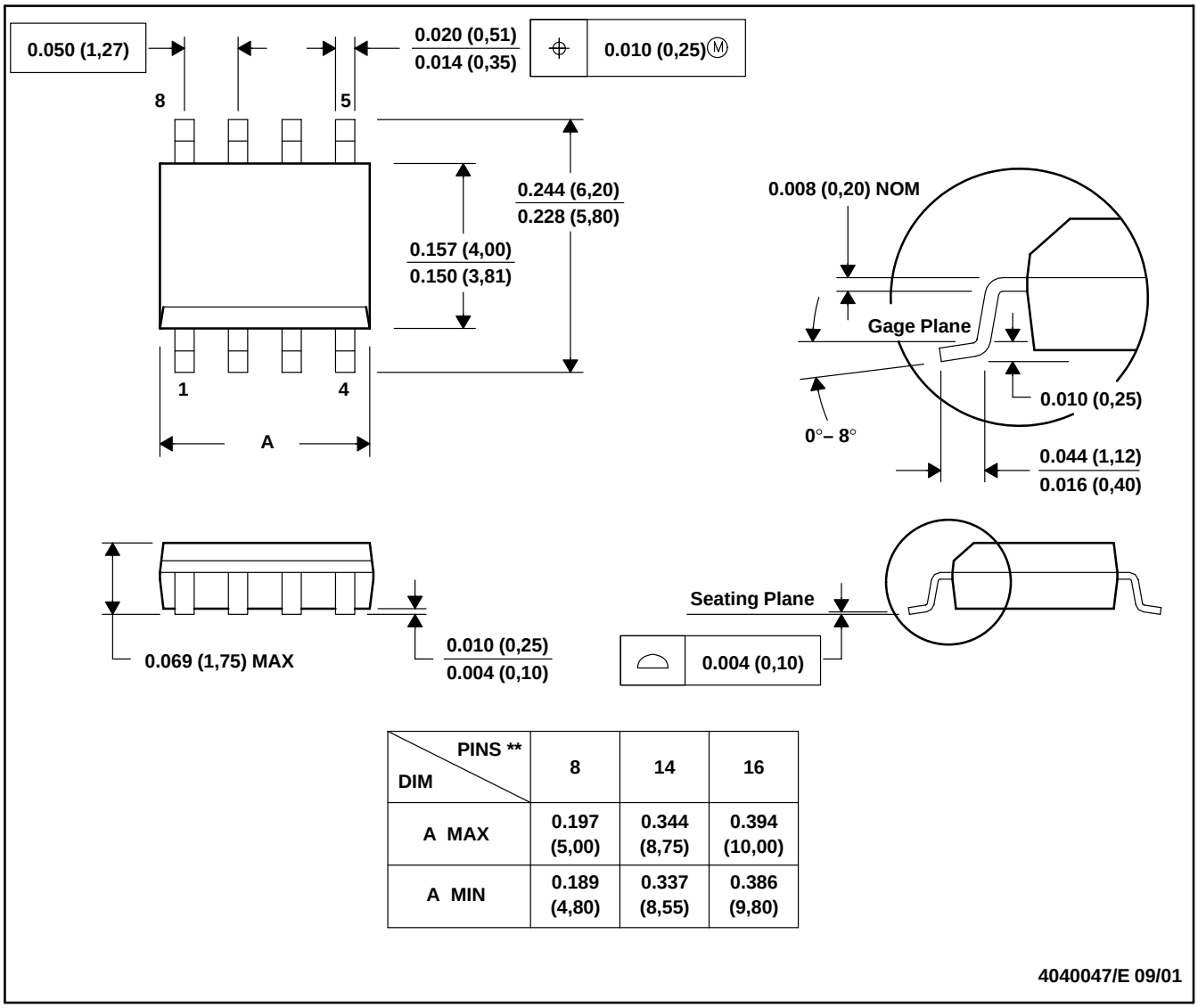
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MSOI002B – JANUARY 1995 – REVISED SEPTEMBER 2001

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

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5.4 CY37256

5V, 3.3V, ISR™ High-Performance CPLDs

Features

- **In-System Reprogrammable™ (ISR™) CMOS CPLDs**
  - **JTAG interface for reconfigurability**
  - **Design changes don't cause pinout changes**
  - **Design changes don't cause timing changes**
- **High density**
  - **32 to 512 macrocells**
  - **32 to 264 I/O pins**
  - **5 dedicated inputs including 4 clock pins**
- **Simple timing model**
  - **No fanout delays**
  - **No expander delays**
  - **No dedicated vs. I/O pin delays**
  - **No additional delay through PIM**
  - **No penalty for using full 16 product terms**
  - **No delay for steering or sharing product terms**
- **3.3V and 5V versions**
- **PCI Compatible**[1]
- **Programmable Bus-Hold capabilities on all I/Os**
- **Intelligent product term allocator provides:**
  - **0 to 16 product terms to any macrocell**
  - **Product term steering on an individual basis**
  - **Product term sharing among local macrocells**
- **Flexible clocking**
  - **4 synchronous clocks per device**
  - **Product Term clocking**
  - **Clock polarity control per logic block**
- **Consistent package/pinout offering across all densities**
  - **Simplifies design migration**
  - **Same pinout for 3.3V and 5.0V devices**
- **Packages**
  - **44 to 400 Leads in PLCC, CLCC, PQFP, TQFP, CQFP, BGA, and Fine-Pitch BGA packages**

General Description

The Ultra37000™ family of CMOS CPLDs provides a range of high-density programmable logic solutions with unparalleled system performance. The Ultra37000 family is designed to bring the flexibility, ease of use, and performance of the 22V10 to high-density CPLDs. The architecture is based on a number of logic blocks that are connected by a Programmable Interconnect Matrix (PIM). Each logic block features its own product term array, product term allocator, and 16 macrocells. The PIM distributes signals from the logic block outputs and all input pins to the logic block inputs.

All of the Ultra37000 devices are electrically erasable and In-System Reprogrammable (ISR), which simplifies both design and manufacturing flows, thereby reducing costs. The ISR feature provides the ability to reconfigure the devices without having design changes cause pinout or timing changes. The Cypress ISR function is implemented through a JTAG-compliant serial interface. Data is shifted in and out through the TDI and TDO pins, respectively. Because of the superior routability and simple timing model of the Ultra37000 devices, ISR allows users to change existing logic designs while simultaneously fixing pinout assignments and maintaining system performance.

The entire family features JTAG for ISR and boundary scan, and is compatible with the PCI Local Bus specification, meeting the electrical and timing requirements. The Ultra37000 family features user programmable bus-hold capabilities on all I/Os.

Ultra37000 5.0V Devices

The Ultra37000 devices operate with a 5V supply and can support 5V or 3.3V I/O levels. V_{CCO} connections provide the capability of interfacing to either a 5V or 3.3V bus. By connecting the V_{CCO} pins to 5V the user insures 5V TTL levels on the outputs. If V_{CCO} is connected to 3.3V the output levels meet 3.3V JEDEC standard CMOS levels and are 5V tolerant. These devices require 5V ISR programming.

Ultra37000V 3.3V Devices

Devices operating with a 3.3V supply require 3.3V on all V_{CCO} pins, reducing the device's power consumption. These devices support 3.3V JEDEC standard CMOS output levels, and are 5V tolerant. These devices allow 3.3V ISR programming.

Note:
1. Due to the 5V-tolerant nature of 3.3V device I/Os, the I/Os are not clamped to V_{CC}, PCI V_{IH}=2V.

Selection Guide

5.0V Selection Guide

General Information

Device	Macrocells	Dedicated Inputs	I/O Pins	Speed (t_{PD})	Speed (f_{MAX})
CY37032	32	5	32	6	200
CY37064	64	5	32/64	6	200
CY37128	128	5	64/128	6.5	167
CY37192	192	5	120	7.5	154
CY37256	256	5	128/160/192	7.5	154
CY37384	384	5	160/192	10	118
CY37512	512	5	160/192/264	10	118

Speed Bins

Device	200	167	154	143	125	100	83	66
CY37032	X		X		X			
CY37064	X		X		X			
CY37128		X			X	X		
CY37192			X		X		X	
CY37256			X		X		X	
CY37384					X		X	
CY37512					X	X	X	

Device-Package Offering & I/O Count

Device	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	160-Lead CQFP	208-Lead PQFP	208-Lead CQFP	256-Lead BGA	352-Lead BGA
CY37032	37	37										
CY37064	37	37	37	69		69						
CY37128				69	69	69	133					
CY37192							125					
CY37256							133	133	165		197	
CY37384									165		197	
CY37512									165	165	197	269

3.3V Selection Guide

General Information

Device	Macrocells	Dedicated Inputs	I/O Pins	Speed (t_{PD})	Speed (f_{MAX})
CY37032V	32	5	32	8.5	143
CY37064V	64	5	32/64	8.5	143
CY37128V	128	5	64/80/128	10	125
CY37192V	192	5	120	12	100
CY37256V	256	5	128/160/192	12	100
CY37384V	384	5	160/192	15	83
CY37512V	512	5	160/192/264	15	83

Speed Bins

Device	200	167	154	143	125	100	83	66
CY37032V				X		X		
CY37064V				X		X		
CY37128V				X	X		X	
CY37192V						X		X
CY37256V				X		X		X
CY37384V							X	X
CY37512V					X		X	X

Shaded areas indicate preliminary speed bins.

Device-Package Offering & I/O Count

Device	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	48-Lead FBGA	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	100-Lead FBGA	160-Lead TQFP	160-Lead CQFP	208-Lead PQFP	208-Lead CQFP	256-Lead BGA	256-Lead FBGA	352-Lead BGA	400-Lead FBGA
CY37032V	37	37		37												
CY37064V	37	37	37	37	69		69	69								
CY37128V					69	69	69	85	133							
CY37192V									125							
CY37256V									133	133	165		197	197		
CY37384V											165		197			
CY37512V											165	165	197		269	269

Architecture Overview of Ultra37000 Family

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) consists of a completely global routing matrix for signals from I/O pins and feedbacks from the logic blocks. The PIM provides extremely robust interconnection to avoid fitting and density limitations.

The inputs to the PIM consist of all I/O and dedicated input pins and all macrocell feedbacks from within the logic blocks. The number of PIM inputs increases with pin count and the number of logic blocks. The outputs from the PIM are signals routed to the appropriate logic blocks. Each logic block receives 36 inputs from the PIM and their complements, allowing for 32-bit operations to be implemented in a single pass through the device. The wide number of inputs to the logic block also improves the routing capacity of the Ultra37000 family.

An important feature of the PIM is its simple timing. The propagation delay through the PIM is accounted for in the timing specifications for each device. There is no additional delay for traveling through the PIM. In fact, all inputs travel through the PIM. As a result, there are no route-dependent timing parameters on the Ultra37000 devices. The worst-case PIM delays are incorporated in all appropriate Ultra37000 specifications.

Routing signals through the PIM is completely invisible to the user. All routing is accomplished by software—no hand routing is necessary. *Warp*™ and third-party development packages automatically route designs for the Ultra37000 family in a matter of minutes. Finally, the rich routing resources of the Ultra37000 family accommodate last minute logic changes while maintaining fixed pin assignments.

Logic Block

The logic block is the basic building block of the Ultra37000 architecture. It consists of a product term array, an intelligent product-term allocator, 16 macrocells, and a number of I/O cells. The number of I/O cells varies depending on the device used. Refer to *Figure 1* for the block diagram.

Product Term Array

Each logic block features a 72 x 87 programmable product term array. This array accepts 36 inputs from the PIM, which originate from macrocell feedbacks and device pins. Active LOW and active HIGH versions of each of these inputs are generated to create the full 72-input field. The 87 product terms in the array can be created from any of the 72 inputs.

Of the 87 product terms, 80 are for general-purpose use for the 16 macrocells in the logic block. Four of the remaining seven product terms in the logic block are output enable (OE) product terms. Each of the OE product terms controls up to eight of the 16 macrocells and is selectable on an individual macrocell basis. In other words, each I/O cell can select between one of two OE product terms to control the output buffer. The first two of these four OE product terms are available to the upper half of the I/O macrocells in a logic block. The other two OE product terms are available to the lower half of the I/O macrocells in a logic block.

The next two product terms in each logic block are dedicated asynchronous set and asynchronous reset product terms. The final product term is the product term clock. The set, reset, OE and product term clock have polarity control to realize OR functions in a single pass through the array.

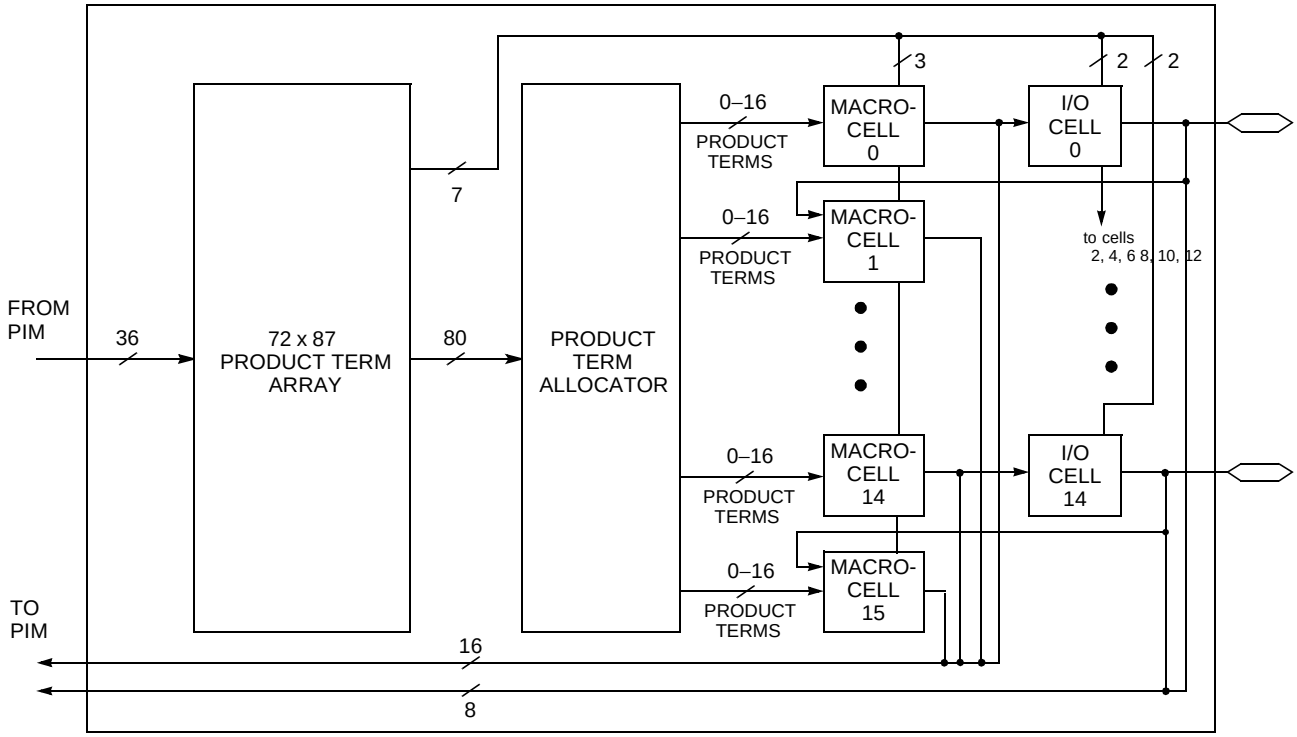


Figure 1. Logic Block with 50% Buried Macrocells

Low-Power Option

Each logic block can operate in high-speed mode for critical path performance, or in low-power mode for power conservation. The logic block mode is set by the user on a logic block by logic block basis.

Product Term Allocator

Through the product term allocator, software automatically distributes product terms among the 16 macrocells in the logic block as needed. A total of 80 product terms are available from the local product term array. The product term allocator provides two important capabilities without affecting performance: product term steering and product term sharing.

Product Term Steering

Product term steering is the process of assigning product terms to macrocells as needed. For example, if one macrocell requires ten product terms while another needs just three, the product term allocator will "steer" ten product terms to one macrocell and three to the other. On Ultra37000 devices, product terms are steered on an individual basis. Any number between 0 and 16 product terms can be steered to any macrocell. Note that 0 product terms is useful in cases where a particular macrocell is unused or used as an input register.

Product Term Sharing

Product term sharing is the process of using the same product term among multiple macrocells. For example, if more than one output has one or more product terms in its equation that are common to other outputs, those product terms are only programmed once. The Ultra37000 product term allocator allows sharing across groups of four output macrocells in a variable fashion. The software automatically takes advantage of this capability—the user does not have to intervene.

Note that neither product term sharing nor product term steering have any effect on the speed of the product. All worst-case steering and sharing configurations have been incorporated in the timing specifications for the Ultra37000 devices.

Ultra37000 Macrocell

Within each logic block there are 16 macrocells. Macrocells can either be I/O Macrocells, which include an I/O Cell which is associated with an I/O pin, or buried Macrocells, which do not connect to an I/O. The combination of I/O Macrocells and buried Macrocells varies from device to device.

Buried Macrocell

Figure 2 displays the architecture of buried macrocells. The buried macrocell features a register that can be configured as combinatorial, a D flip-flop, a T flip-flop, or a level-triggered latch.

The register can be asynchronously set or asynchronously reset at the logic block level with the separate set and reset product terms. Each of these product terms features programmable polarity. This allows the registers to be set or reset based on an AND expression or an OR expression.

Clocking of the register is very flexible. Four global synchronous clocks and a product term clock are available to clock the register. Furthermore, each clock features programmable polarity so that registers can be triggered on falling as well as rising edges (see the Clocking section). Clock polarity is chosen at the logic block level.

The buried macrocell also supports input register capability. The buried macrocell can be configured to act as an input register (D-type or latch) whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

I/O Macrocell

Figure 2 illustrates the architecture of the I/O macrocell. The I/O macrocell supports the same functions as the buried macrocell with the addition of I/O capability. At the output of the macrocell, a polarity control mux is available to select active LOW or active HIGH signals. This has the added advantage of allowing significant logic reduction to occur in many applications.

The Ultra37000 macrocell features a feedback path to the PIM separate from the I/O pin input path. This means that if the macrocell is buried (fed back internally only), the associated I/O pin can still be used as an input.

Bus Hold Capabilities on all I/Os

Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold maintains the last state of a pin when the pin is placed in a high-impedance state, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND. For more information, see the application note "Understanding Bus-Hold – A Feature of Cypress CPLDs."

Programmable Slew Rate Control

Each output has a programmable configuration bit, which sets the output slew rate to fast or slow. For designs concerned with meeting FCC emissions standards the slow edge provides for lower system noise. For designs requiring very high performance the fast edge rate provides maximum system performance.

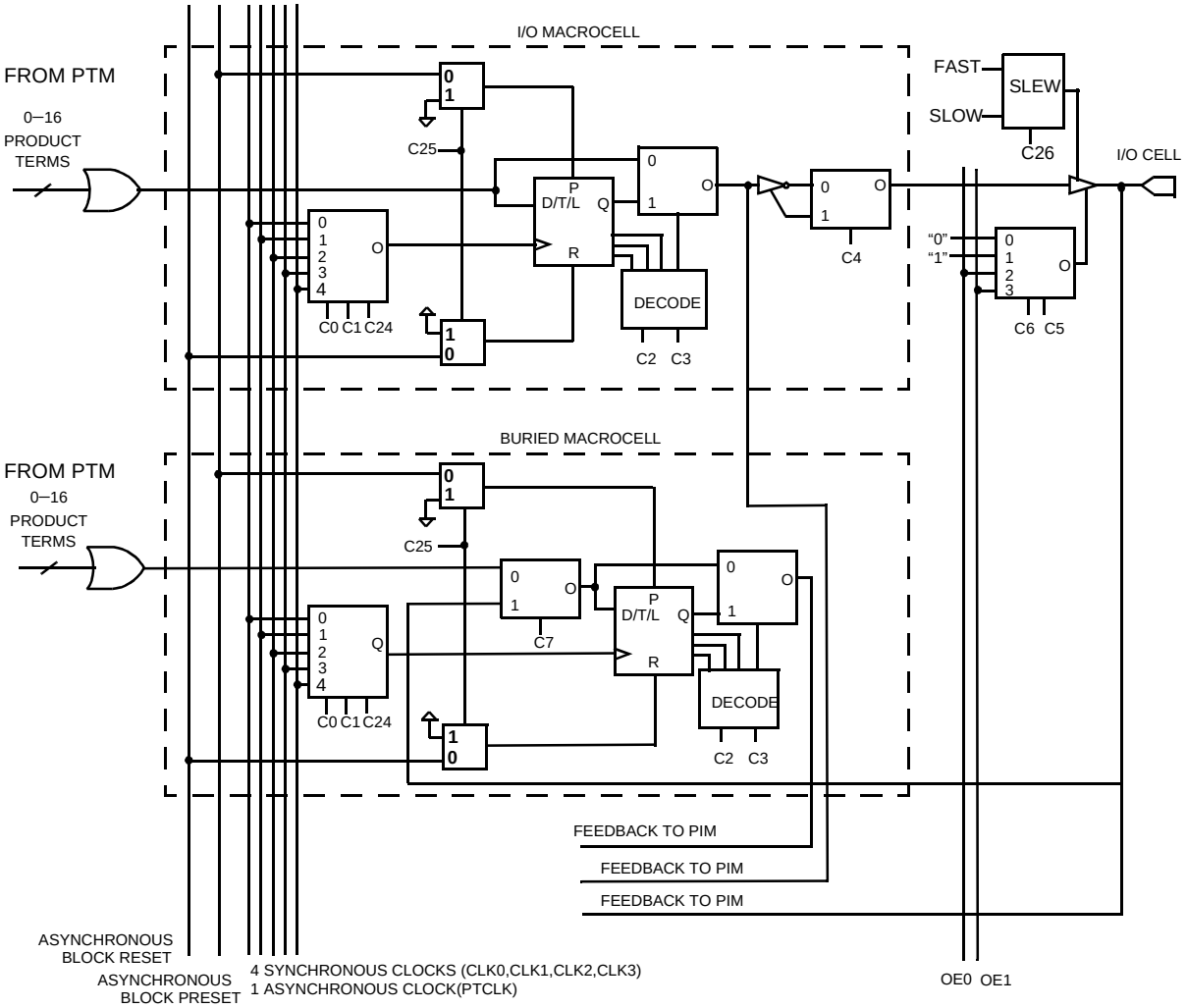


Figure 2. I/O and Buried Macrocells

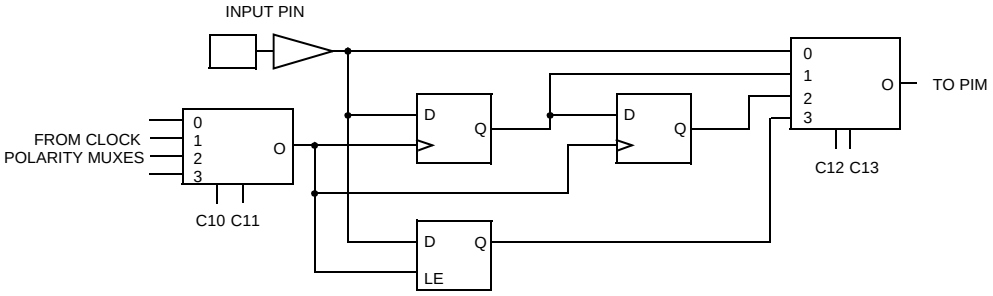


Figure 3. Input Macrocell

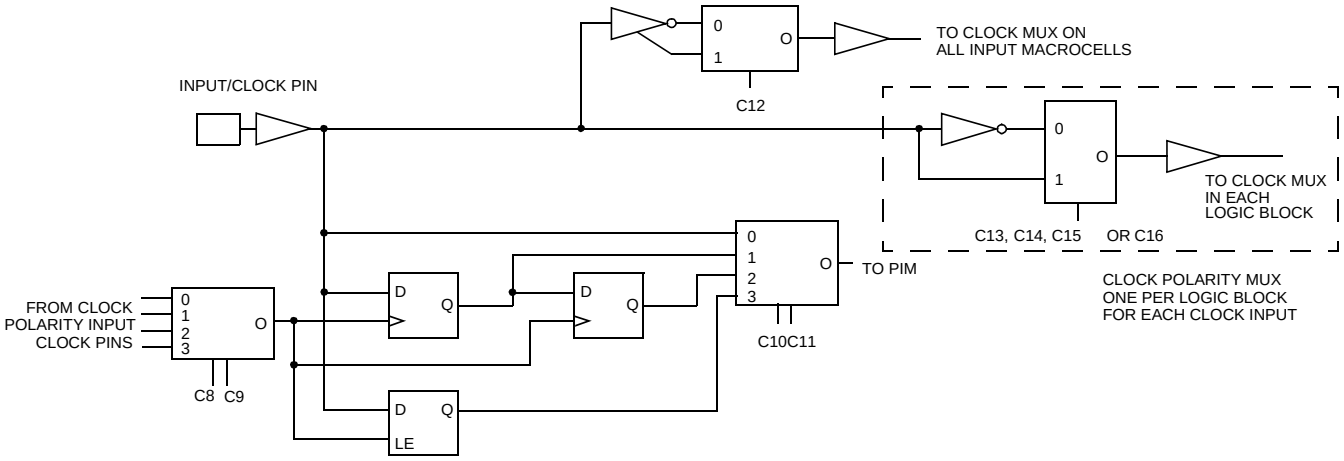


Figure 4. Input/Clock Macrocell

Clocking

Each I/O and buried macrocell has access to four synchronous clocks (CLK0, CLK1, CLK2 and CLK3) as well as an asynchronous product term clock PTCLK. Each input macrocell has access to all four synchronous clocks.

Dedicated Inputs/Clocks

Five pins on each member of the Ultra37000 family are designated as input-only. There are two types of dedicated inputs on Ultra37000 devices: input pins and input/clock pins. *Figure 3* illustrates the architecture for input pins. Four input options are available for the user: combinatorial, registered, double-registered, or latched. If a registered or latched option is selected, any one of the input clocks can be selected for control.

Figure 4 illustrates the architecture for the input/clock pins. Like the input pins, input/clock pins can be combinatorial, registered, double-registered, or latched. In addition, these pins feed the clocking structures throughout the device. The clock path at the input has user-configurable polarity.

Product Term Clocking

In addition to the four synchronous clocks, the Ultra37000 family also has a product term clock for asynchronous clocking. Each logic block has an independent product term clock which is available to all 16 macrocells. Each product term clock also supports user configurable polarity selection.

Timing Model

One of the most important features of the Ultra37000 family is the simplicity of its timing. All delays are worst case and system performance is unaffected by the features used. *Figure 5* illustrates the true timing model for the 167-MHz devices in high speed mode. For combinatorial paths, any input to any output incurs a 6.5-ns worst-case delay regardless of the amount of logic used. For synchronous systems, the input set-up time to the output macrocells for any input is 3.5 ns and the clock to output time is also 4.0 ns. These measurements are for any output and synchronous clock, regardless of the logic used.

The Ultra37000 features:

- No fanout delays
- No expander delays
- No dedicated vs. I/O pin delays
- No additional delay through PIM
- No penalty for using 0–16 product terms
- No added delay for steering product terms
- No added delay for sharing product terms
- No routing delays
- No output bypass delays

The simple timing model of the Ultra37000 family eliminates unexpected performance penalties.

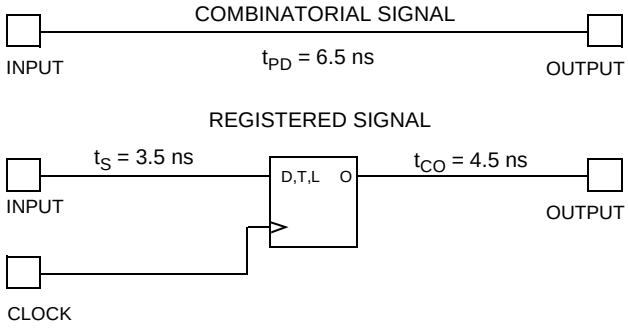


Figure 5. Timing Model for CY37128

JTAG and PCI Standards

PCI Compliance

5V operation of the Ultra37000 is fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The 3.3V products meet all PCI requirements except for the output 3.3V clamp, which is in direct conflict with 5V tolerance. The Ultra37000 family's simple and predictable timing model ensures compliance with the PCI AC specifications independent of the design.

IEEE 1149.1 Compliant JTAG

The Ultra37000 family has an IEEE 1149.1 JTAG interface for both Boundary Scan and ISR.

Boundary Scan

The Ultra37000 family supports Bypass, Sample/Preload, Extest, Idcode, and Usercode boundary scan instructions. The JTAG interface is shown in *Figure 6*.

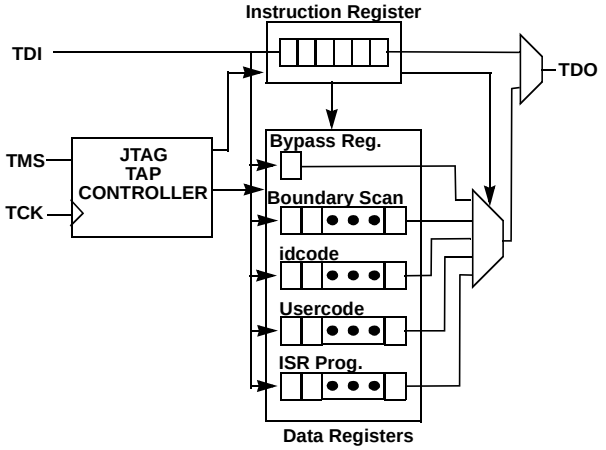


Figure 6. JTAG Interface

In-System Reprogramming (ISR)

In-System Reprogramming is the combination of the capability to program or reprogram a device on-board, and the ability to support design changes without changing the system timing or device pinout. This combination means design changes during debug or field upgrades do not cause board respins. The Ultra37000 family implements ISR by providing a JTAG compliant interface for on-board programming, robust routing resources for pinout flexibility, and a simple timing model for consistent system performance.

Development Software Support

Warp™

Warp is a state-of-the-art compiler and complete CPLD design tool. For design entry, *Warp* provides an IEEE-STD-1076/1164 VHDL text editor, an IEEE-STD-1364 Verilog text editor, and a graphical finite state machine editor. It provides optimized synthesis and fitting by replacing basic circuits with ones pre-optimized for the target device, by implementing logic in unused memory and by perfect communication between fitting and synthesis. To facilitate design and debugging, *Warp* provides graphical timing simulation and analysis.

Warp Professional™

Warp Professional contains several additional features. It provides an extra method of design entry with its graphical block diagram editor. It allows up to 5 ms timing simulation instead of only 2 ms. It allows comparison of waveforms before and after design changes.

Warp Enterprise™

Warp Enterprise provides even more features. It provides unlimited timing simulation and source-level behavioral simulation as well as a debugger. It has the ability to generate graphical HDL blocks from HDL text. It can even generate testbenches.

Warp is available for PC and UNIX platforms. Some features are not available in the UNIX version. For further information see the *Warp* for PC, *Warp* for UNIX, *Warp* Professional and *Warp* Enterprise data sheets on Cypress's web site (www.cypress.com).

Third-Party Software

Although *Warp* is a complete CPLD development tool on its own, it interfaces with nearly every third party EDA tool. All major third-party software vendors provide support for the Ultra37000 family of devices. Refer to the third-party software data sheet or contact your local sales office for a list of currently supported third-party vendors.

Programming

There are four programming options available for Ultra37000 devices. The first method is to use a PC with the 37000 UltraISR programming cable and software. With this method, the ISR pins of the Ultra37000 devices are routed to a connector at the edge of the printed circuit board. The 37000 UltraISR programming cable is then connected between the parallel port of the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on each of the Ultra37000 devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish the programming, reading, verifying, and other ISR functions. For more information on the Cypress ISR Interface, see the ISR Programming Kit data sheet (CY3700i).

The second method for programming Ultra37000 devices is on automatic test equipment (ATE). This is accomplished through a file created by the ISR software. Check the Cypress website for the latest ISR software download information.

The third programming option for Ultra37000 devices is to utilize the embedded controller or processor that already exists in the system. The Ultra37000 ISR software assists in this method by converting the device JEDEC maps into the ISR serial stream that contains the ISR instruction information and the addresses and data of locations to be programmed. The embedded controller then simply directs this ISR stream to the chain of Ultra37000 devices to complete the desired reconfiguring or diagnostic operations. Contact your local sales office for information on availability of this option.

The fourth method for programming Ultra37000 devices is to use the same programmer that is currently being used to program FLASH370i devices.

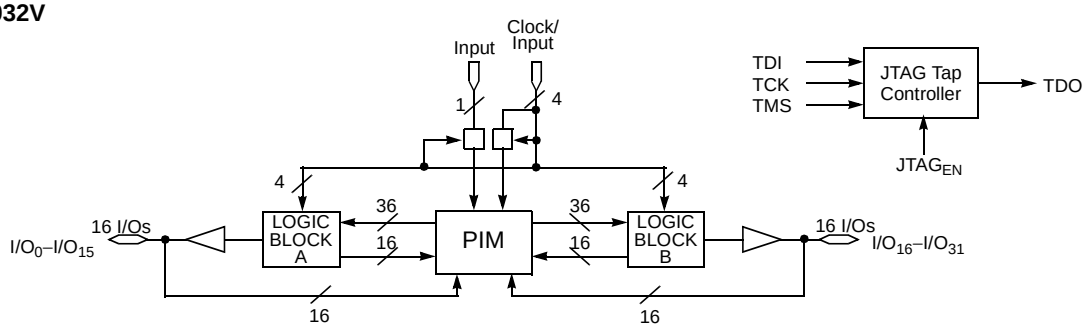
For all pinout, electrical, and timing requirements, refer to device data sheets. For ISR cable and software specifications, refer to the UltraISR kit data sheet (CY3700i).

Third-Party Programmers

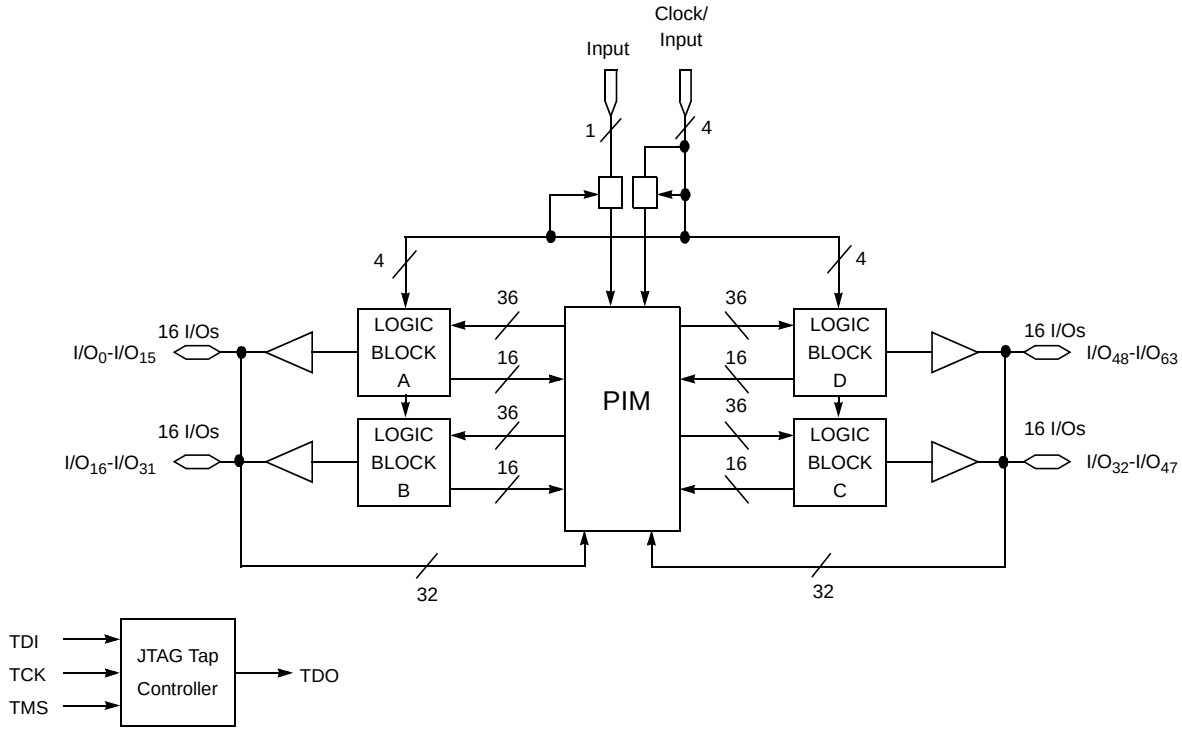
As with development software, Cypress support is available on a wide variety of third-party programmers. All major third-party programmers (including BP Micro, Data I/O, and SMS) support the Ultra37000 family.

Logic Block Diagrams

CY37032 / CY37032V

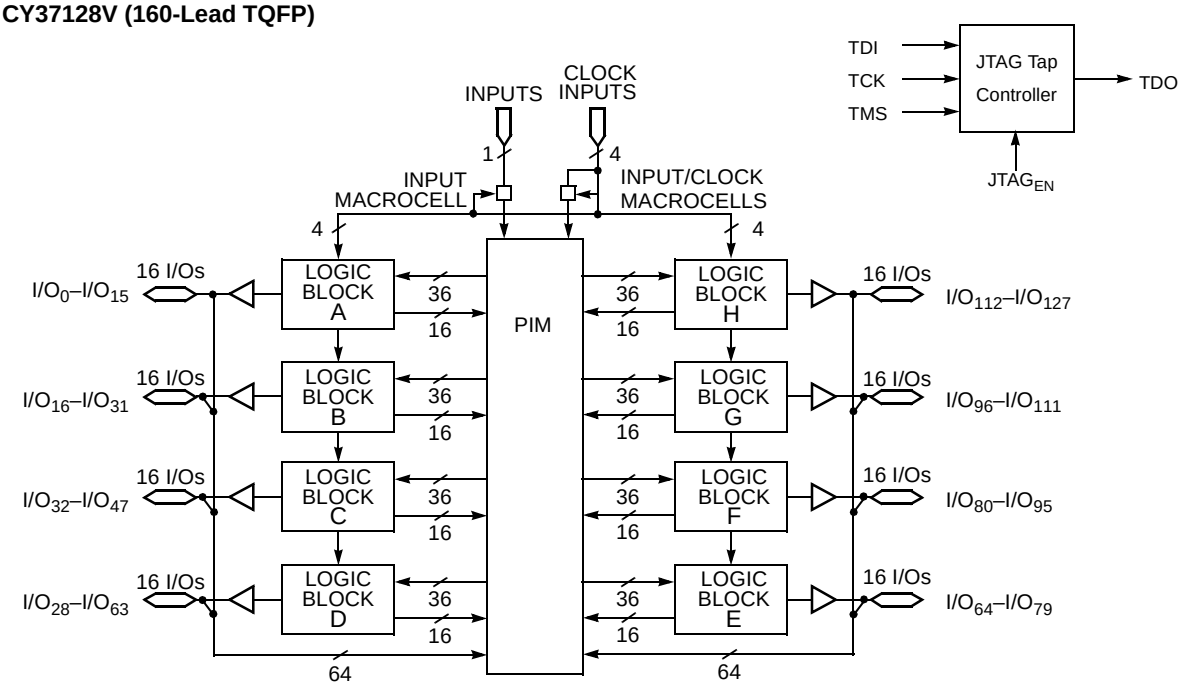


CY37064 / CY37064V (100-Lead TQFP)

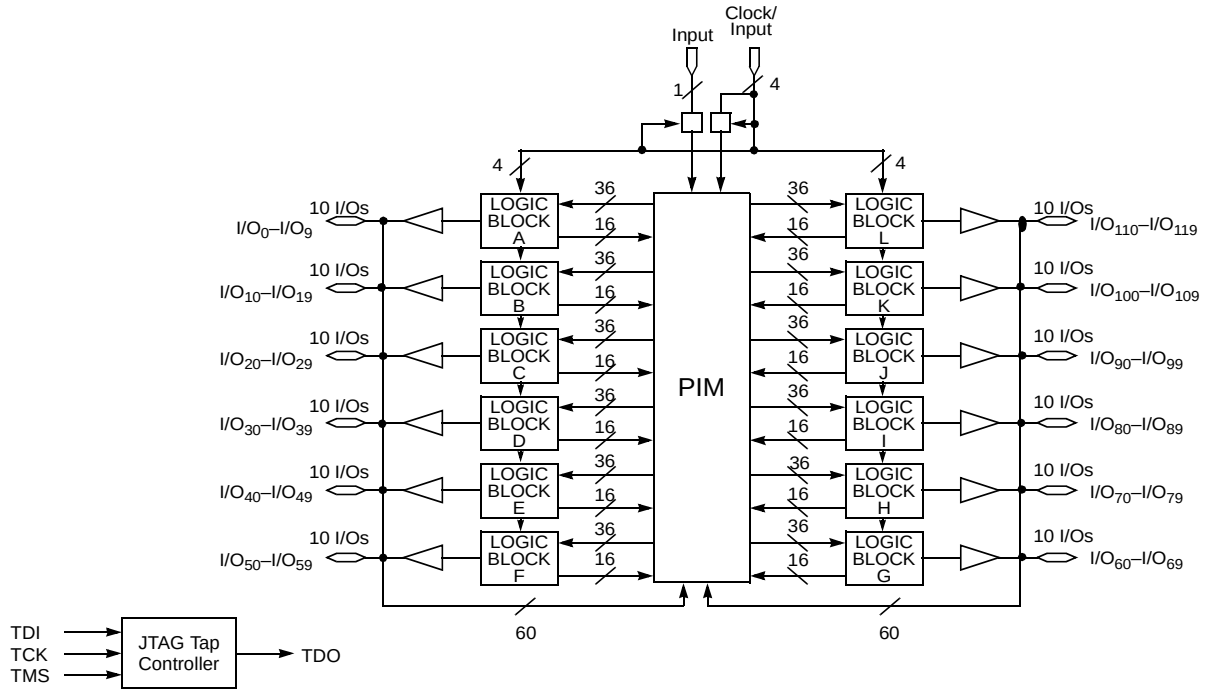


Logic Block Diagrams (continued)

CY37128 / CY37128V (160-Lead TQFP)

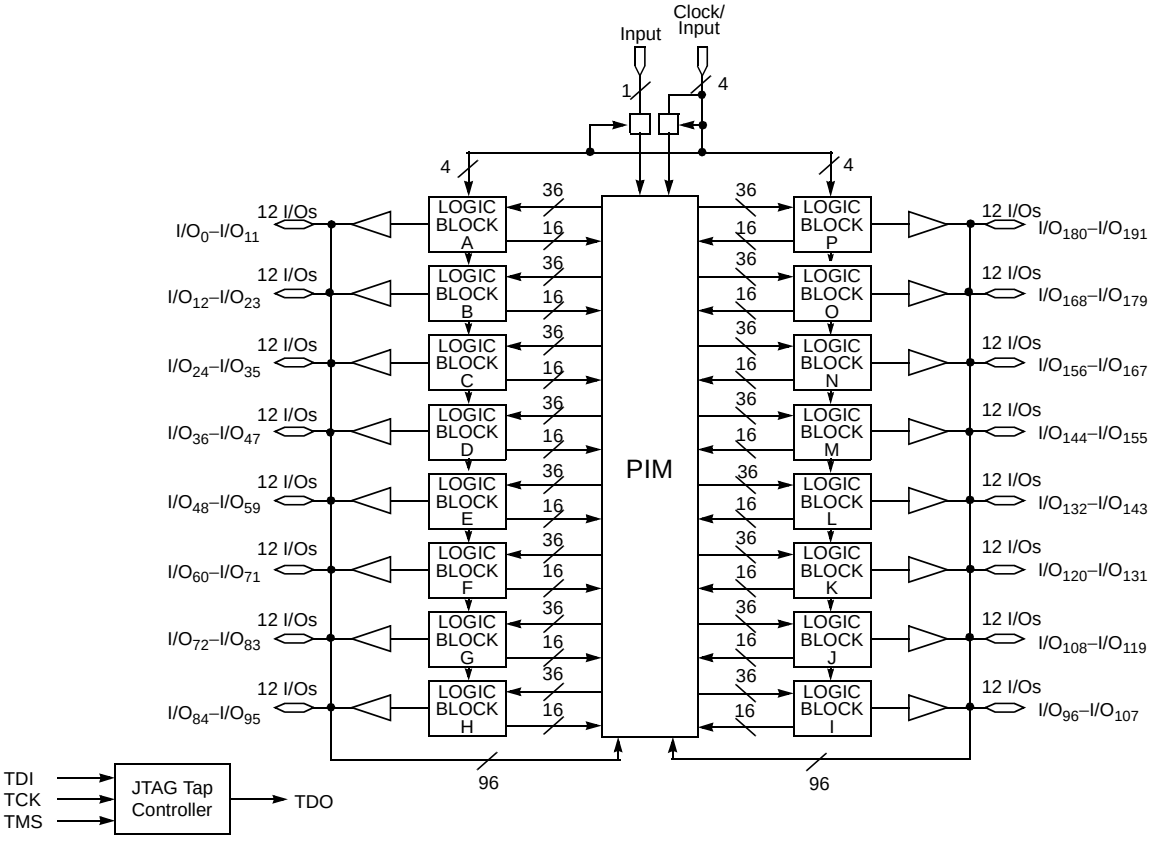


CY37192 / CY37192V (160-Lead TQFP)



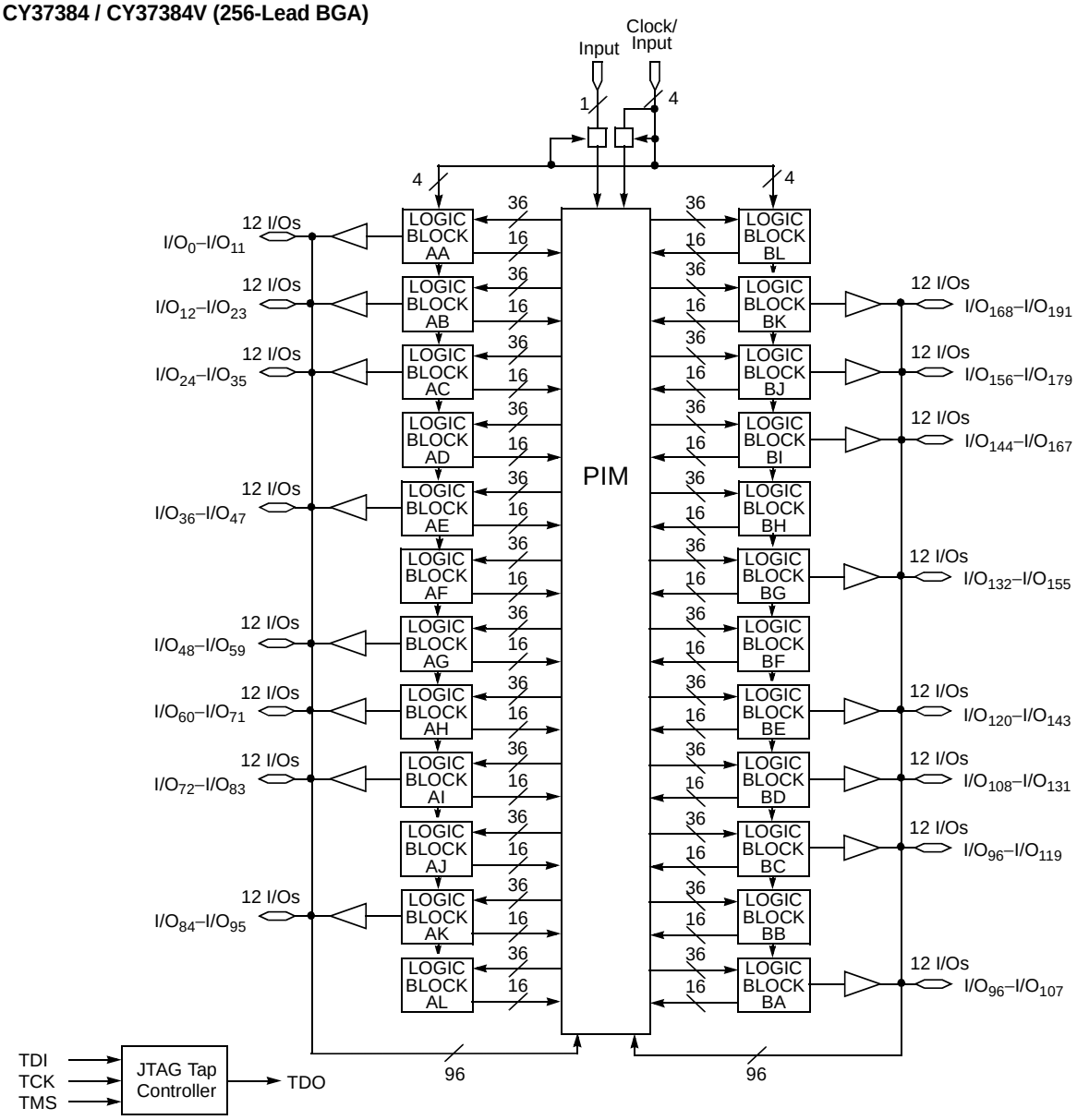
Logic Block Diagrams (continued)

CY37256 / CY37256V (256-Lead BGA)



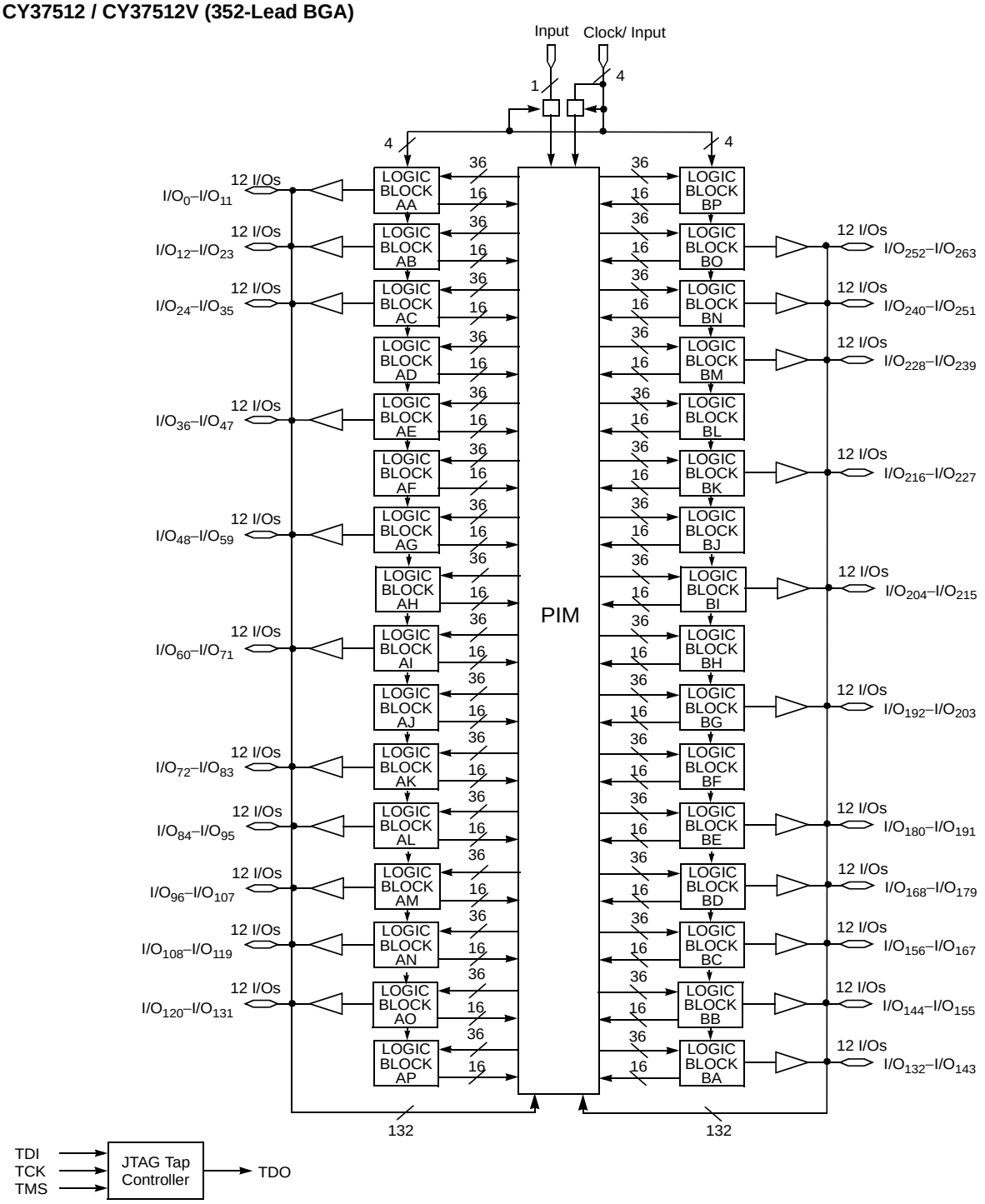
Logic Block Diagrams (continued)

CY37384 / CY37384V (256-Lead BGA)



Logic Block Diagrams (continued)

CY37512 / CY37512V (352-Lead BGA)



5.0V Device Characteristics

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

DC Program Voltage ..... 4.5 to 5.5V

Current into Outputs ..... 16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Junction Temperature	Output Condition	V_{CC}	V_{CCO}
Commercial	0°C to +70°C	0°C to +90°C	5V	5V ± 0.25V	5V ± 0.25V
			3.3V	5V ± 0.25V	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to +105°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V
Military[3]	–55°C to +125°C	–55°C to +130°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V

Notes:

2. Normal Programming Conditions apply across Ambient Temperature Range for specified programming methods. For more information on programming the Ultra37000 Family devices, please refer to the Application Note titled “An Introduction to In System Reprogramming with the Ultra37000.”
3. T_A is the “Instant On” case temperature.

5.0V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3.2 mA (Com'l/Ind)[4]	2.4			V
			I_{OH} = –2.0 mA (Mil)[4]	2.4			V
V_{OHZ}	Output HIGH Voltage with Output Disabled[5]	V_{CC} = Max.	I_{OH} = 0 µA (Com'l)[6]			4.2	V
			I_{OH} = 0 µA (Ind/Mil)[6]			4.5	V
			I_{OH} = –100 µA (Com'l)[6]			3.6	V
			I_{OH} = –150 µA (Ind/Mil)[6]			3.6	V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA (Com'l/Ind)[4]			0.5	V
			I_{OL} = 12 mA (Mil)[4]			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[7]		2.0		V_{CCmax}	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[7]		–0.5		0.8	V
I_{IX}	Input Load Current	V_I = GND OR V_{CC}, Bus-Hold Disabled		–10		10	µA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled, Bus-Hold Disabled		–50		50	µA
I_{OS}	Output Short Circuit Current[8, 5]	V_{CC} = Max., V_{OUT} = 0.5V		–30		–160	mA
I_{BHL}	Input Bus-Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75			µA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75			µA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current	V_{CC} = Max.				+500	µA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current	V_{CC} = Max.				–500	µA

Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 5.0V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	10	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual Function Pins[9]	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

Notes:

4. I_{OH} = –2 mA, I_{OL} = 2 mA for TDO.
5. Tested initially and after any design or process changes that may affect these parameters.
6. When the I/O is output disabled, the bus-hold circuit can weakly pull the I/O to above 3.6V if no leakage current is allowed. Note that all I/Os are output disabled during ISR programming. Refer to the application note "Understanding Bus-Hold" for additional information.
7. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
8. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
9. Dual pins are I/O with JTAG pins.

3.3V Device Characteristics

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

DC Program Voltage ..... 3.0 to 3.6V

Current into Outputs ..... 8 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Junction Temperature	V_{CC}
Commercial	0°C to +70°C	0°C to +90°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to +105°C	3.3V ± 0.3V
Military[3]	–55°C to +125°C	–55°C to +130°C	3.3V ± 0.3V

3.3V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –4 mA (Com'l)[4]	2.4		V
			I_{OH} = –3 mA (Mil)[4]			
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8 mA (Com'l)[4]		0.5	V
			I_{OL} = 6 mA (Mil)[4]			
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[7]		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[7]		–0.5	0.8	V
I_{IX}	Input Load Current	V_I = GND OR V_{CC}, Bus-Hold Disabled		–10	10	µA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled, Bus-Hold Disabled		–50	50	µA
I_{OS}	Output Short Circuit Current[8, 5]	V_{CC} = Max., V_{OUT} = 0.5V		–30	–160	mA
I_{BHL}	Input Bus-Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75		µA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75		µA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current	V_{CC} = Max.			+500	µA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current	V_{CC} = Max.			–500	µA

Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 3.3V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

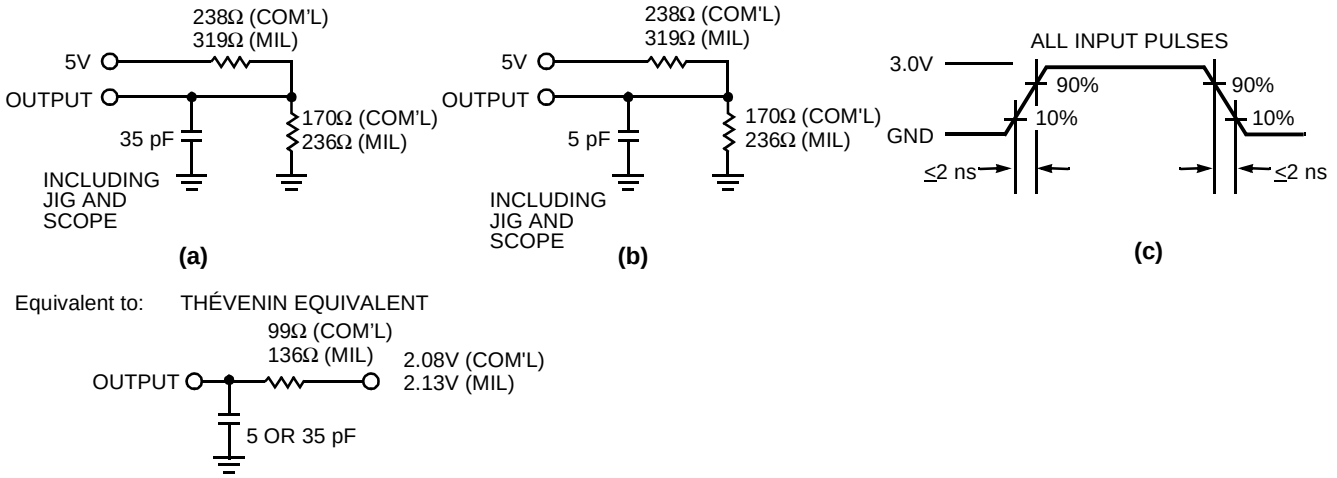
Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	8	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual Functional Pins[9]	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

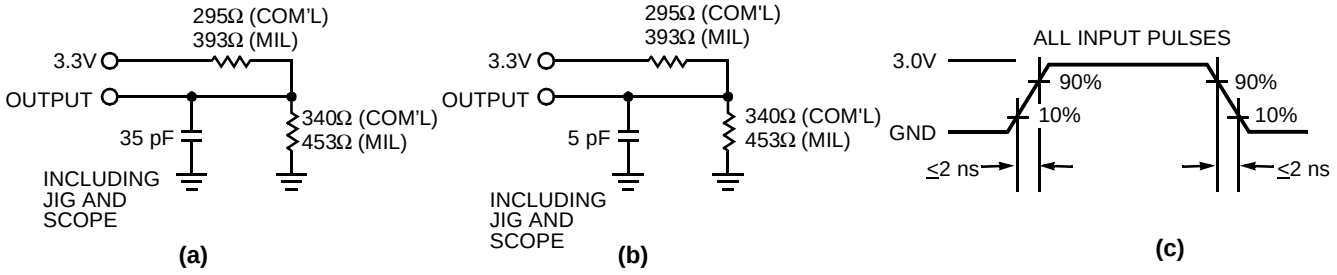
AC Characteristics.

5.0V AC Test Loads and Waveforms

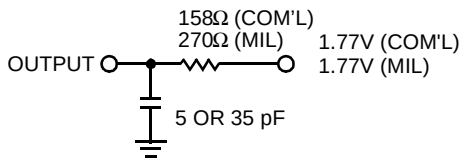


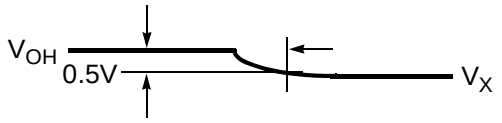
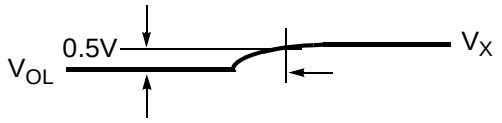
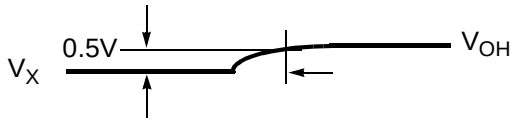
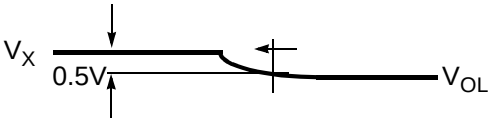
Equivalent to: THÉVENIN EQUIVALENT

3.3V AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Parameter[10]	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	1.5V	
$t_{EA(-)}$	V_{the}	

(d) Test Waveforms

Note:
10. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.

Switching Characteristics Over the Operating Range[11]

Parameter	Description	Unit
Combinatorial Mode Parameters		
t_{PD}[12, 13, 14]	Input to Combinatorial Output	ns
t_{PDL}[12, 13, 14]	Input to Output Through Transparent Input or Output Latch	ns
t_{PDLL}[12, 13, 14]	Input to Output Through Transparent Input and Output Latches	ns
t_{EA}[12, 13, 14]	Input to Output Enable	ns
t_{ER}[10, 12]	Input to Output Disable	ns
Input Register Parameters		
t_{WL}	Clock or Latch Enable Input LOW Time[8]	ns
t_{WH}	Clock or Latch Enable Input HIGH Time[8]	ns
t_{IS}	Input Register or Latch Set-Up Time	ns
t_{IH}	Input Register or Latch Hold Time	ns
t_{ICO}[12, 13, 14]	Input Register Clock or Latch Enable to Combinatorial Output	ns
t_{ICOL}[12, 13, 14]	Input Register Clock or Latch Enable to Output Through Transparent Output Latch	ns
Synchronous Clocking Parameters		
t_{CO}[13, 14]	Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output	ns
t_{S}[12]	Set-Up Time from Input to Sync. Clk (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	ns
t_{H}	Register or Latch Data Hold Time	ns
t_{CO2}[12, 13, 14]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Combinatorial Output Delay (Through Logic Array)	ns
t_{SCS}[12]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable (Through Logic Array)	ns
t_{SL}[12]	Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock (CLK_0 CLK_1, CLK_2, or CLK_3) or Latch Enable	ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	ns
Product Term Clocking Parameters		
t_{COPT}[12, 13, 14]	Product Term Clock or Latch Enable (PTCLK) to Output	ns
t_{SPT}	Set-Up Time from Input to Product Term Clock or Latch Enable (PTCLK)	ns
t_{HPT}	Register or Latch Data Hold Time	ns
t_{ISPT}[12]	Set-Up Time for Buried Register used as an Input Register from Input to Product Term Clock or Latch Enable (PTCLK)	ns
t_{IHPT}	Buried Register Used as an Input Register or Latch Data Hold Time	ns
t_{CO2PT}[12, 13, 14]	Product Term Clock or Latch Enable (PTCLK) to Output Delay (Through Logic Array)	ns
Pipelined Mode Parameters		
t_{ICS}[12]	Input Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) to Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3)	ns

Notes:
11. All AC parameters are measured with two outputs switching and 35-pF AC Test Load.
12. Logic Blocks operating in Low-Power Mode, add t_{LP} to this spec.
13. Outputs using Slow Output Slew Rate, add t_{SLEW} to this spec.
14. When V_{CCO}= 3.3V, add $t_{3.3IO}$ to this spec.

Switching Characteristics Over the Operating Range[11] (continued)

Parameter	Description	Unit
Operating Frequency Parameters		
f_{MAX1}	Maximum Frequency with Internal Feedback (Lesser of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[5]	MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)[5]	MHz
f_{MAX3}	Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ or $1/(t_{WL} + t_{WH})$[5]	MHz
f_{MAX4}	Maximum Frequency in Pipelined Mode (Lesser of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)[5]	MHz
Reset/Preset Parameters		
t_{RW}	Asynchronous Reset Width[5]	ns
t_{RR}[12]	Asynchronous Reset Recovery Time[5]	ns
t_{RO}[12, 13, 14]	Asynchronous Reset to Output	ns
t_{PW}	Asynchronous Preset Width[5]	ns
t_{PR}[12]	Asynchronous Preset Recovery Time[5]	ns
t_{PO}[12, 13, 14]	Asynchronous Preset to Output	ns
User Option Parameters		
t_{LP}	Low Power Adder	ns
t_{SLEW}	Slow Output Slew Rate Adder	ns
$t_{3.3IO}$	3.3V I/O Mode Timing Adder[5]	ns
JTAG Timing Parameters		
$t_{S\ JTAG}$	Set-Up Time from TDI and TMS to TCK[5]	ns
$t_{H\ JTAG}$	Hold Time on TDI and TMS[5]	ns
$t_{CO\ JTAG}$	Falling Edge of TCK to TDO[5]	ns
f_{JTAG}	Maximum JTAG Tap Controller Frequency[5]	ns

Switching Characteristics Over the Operating Range[11]

Parameter	200 MHz		167 MHz		154 MHz		143 MHz		125 MHz		100 MHz		83 MHz		66 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters																	
t_{PD}[12, 13, 14]		6		6.5		7.5		8.5		10		12		15		20	ns
t_{PDL}[12, 13, 14]		11		12.5		14.5		16		16.5		17		19		22	ns
t_{PDLL}[12, 13, 14]		12		13.5		15.5		17		17.5		18		20		24	ns
t_{EA}[12, 13, 14]		8		8.5		11		13		14		16		19		24	ns
t_{ER}[10, 12]		8		8.5		11		13		14		16		19		24	ns
Input Register Parameters																	
t_{WL}	2.5		2.5		2.5		2.5		3		3		4		5		ns
t_{WH}	2.5		2.5		2.5		2.5		3		3		4		5		ns
t_{IS}	2		2		2		2		2		2.5		3		4		ns
t_{IH}	2		2		2		2		2		2.5		3		4		ns
t_{ICO}[12, 13, 14]		11		11		11		12.5		12.5		16		19		24	ns
t_{ICOL}[12, 13, 14]		12		12		12		14		16		18		21		26	ns
Synchronous Clocking Parameters																	
t_{CO}[13, 14]		4		4		4.5		6		6.5[15]		6.5[16]		8[17]		10	ns
t_{S}[12]	4		4		5		5		5.5[15]		6[16]		8[17]		10		ns
t_{H}	0		0		0		0		0		0		0		0		ns
t_{CO2}[12, 13, 14]		9.5		10		11		12		14		16		19		24	ns
t_{SCS}[12]	5		6		6.5		7		8[15]		10		12		15		ns
t_{SL}[12]	7.5		7.5		8.5		9		10		12		15		15		ns
t_{HL}	0		0		0		0		0		0		0		0		ns
Product Term Clocking Parameters																	
t_{COPT}[12, 13, 14]		7		10		10		13		13		13		15		20	ns
t_{SPT}	2.5		2.5		2.5		3		5		5.5		6		7		ns
t_{HPT}	2.5		2.5		2.5		3		5		5.5		6		7		ns
t_{ISPT}[12]	0		0		0		0		0		0		0		0		ns
t_{IHPT}	6		6.5		6.5		7.5		9		11		14		19		ns
t_{CO2PT}[12, 13, 14]		12		14		15		19		19		21		24		30	ns
Pipelined Mode Parameters																	
t_{ICS}[12]	5		6		6		7		8[15]		10		12		15		ns
Operating Frequency Parameters																	
f_{MAX1}	200		167		154		143		125[15]		100		83		66		MHz
f_{MAX2}	200		200		200		167		154		153[16]		125[17]		100		MHz
f_{MAX3}	125		125		105		91		83		80[16]		62.5		50		MHz
f_{MAX4}	167		167		154		125		118		100		83		66		MHz

Notes:

15. The following values correspond to the CY37512 and CY37384 devices: t_{CO} = 5 ns, t_S = 6.5 ns, t_{SCS} = 8.5 ns, t_{ICS} = 8.5 ns, f_{MAX1} = 118 MHz.
16. The following values correspond to the CY37192V and CY37256V devices: t_{CO} = 6 ns, t_S = 7 ns, f_{MAX2} = 143 MHz, f_{MAX3} = 77 MHz, and f_{MAX4} = 100 MHz; and for the CY37512 devices: t_S = 7 ns.
17. The following values correspond to the CY37512V and CY37384V devices: t_{CO} = 6.5 ns, t_S = 9.5 ns, and f_{MAX2} = 105 MHz.

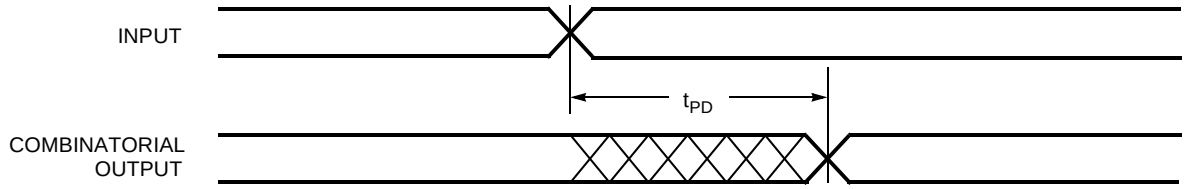
Switching Characteristics Over the Operating Range[11] (continued)

Parameter	200 MHz		167 MHz		154 MHz		143 MHz		125 MHz		100 MHz		83 MHz		66 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Preset Parameters																	
t_{RW}	8		8		8		8		10		12		15		20		ns
t_{RR}[12]	10		10		10		10		12		14		17		22		ns
t_{RO}[12, 13, 14]		12		13		13		14		15		18		21		26	ns
t_{PW}	8		8		8		8		10		12		15		20		ns
t_{PR}[12]	10		10		10		10		12		14		17		22		ns
t_{PO}[12, 13, 14]		12		13		13		14		15		18		21		26	ns
User Option Parameters																	
t_{LP}		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
t_{SLEW}		3		3		3		3		3		3		3		3	ns
$t_{3.3IO}$[18]		0.3		0.3		0.3		0.3		0.3		0.3		0.3		0.3	ns
JTAG Timing Parameters																	
$t_{S\ JTAG}$	0		0		0		0		0		0		0		0		ns
$t_{H\ JTAG}$	20		20		20		20		20		20		20		20		ns
$t_{CO\ JTAG}$		20		20		20		20		20		20		20		20	ns
f_{JTAG}		20		20		20		20		20		20		20		20	MHz

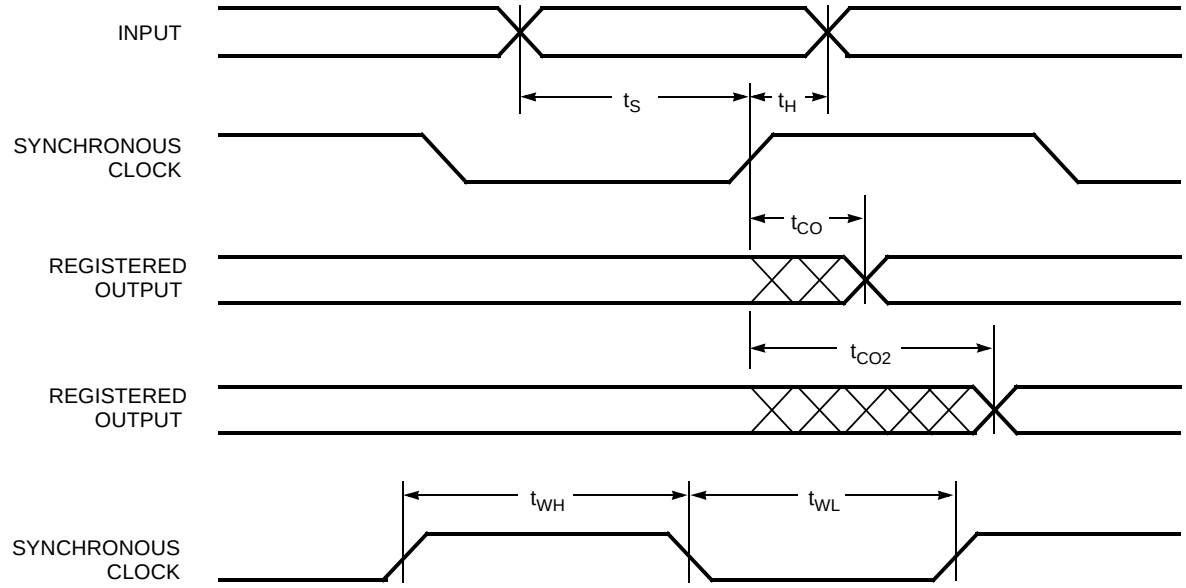
Note:
18. Only applicable to the 5V devices.

Switching Waveforms

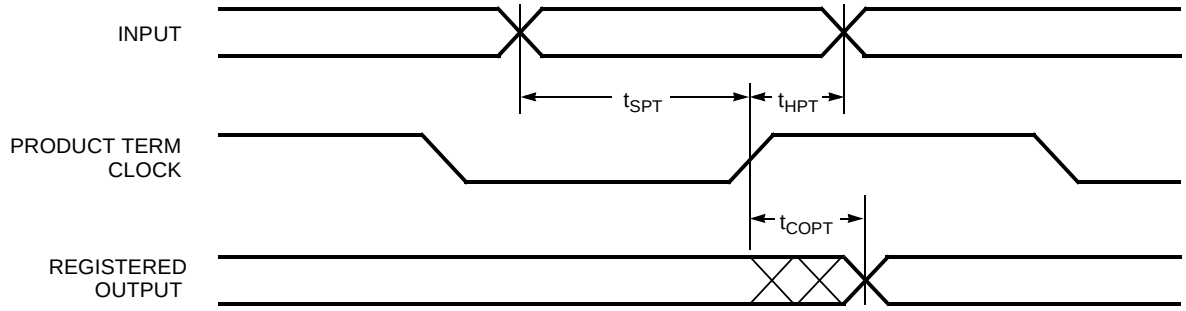
Combinatorial Output



Registered Output with Synchronous Clocking

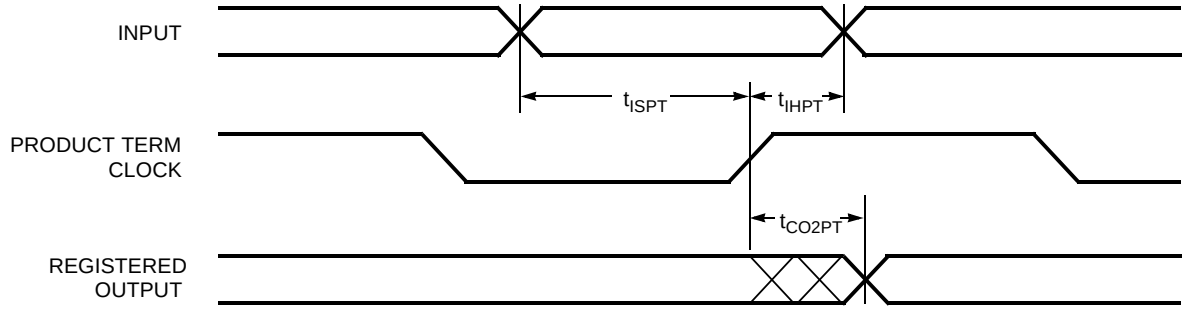


Registered Output with Product Term Clocking Input Going Through the Array

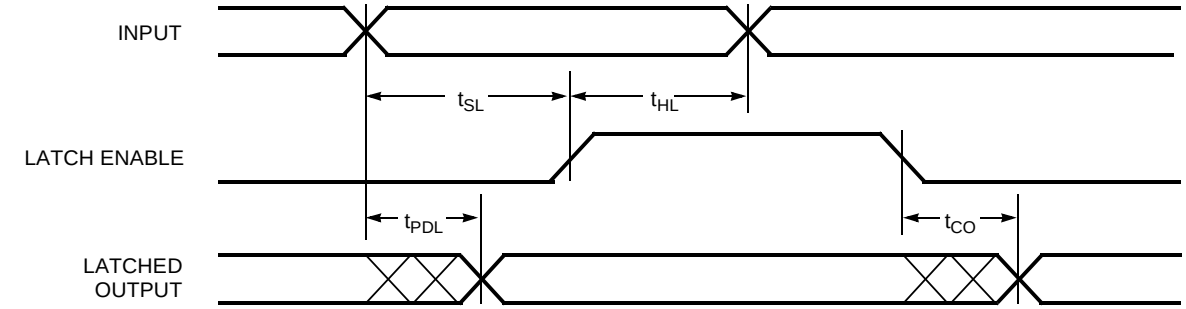


Switching Waveforms (continued)

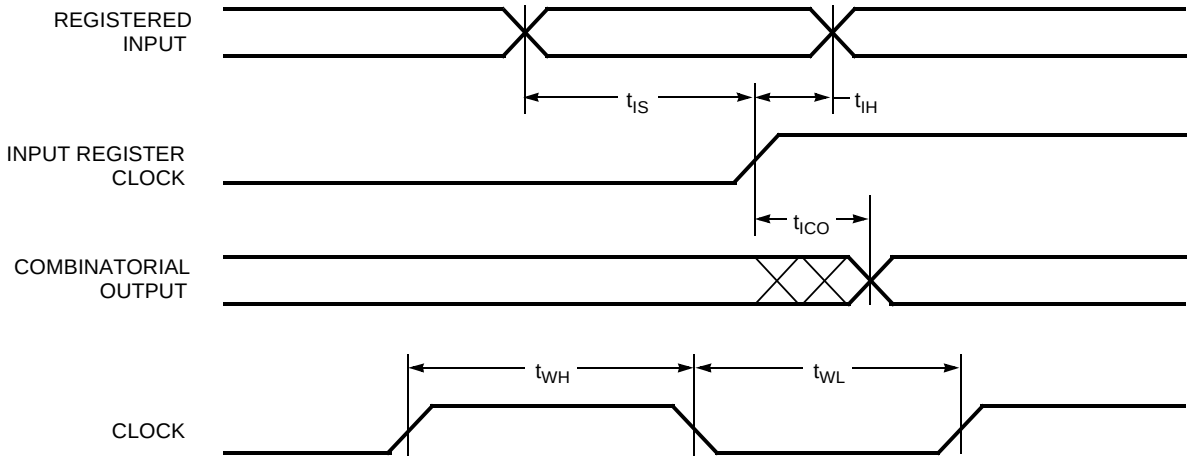
Registered Output with Product Term Clocking Input Coming From Adjacent Buried Register



Latched Output

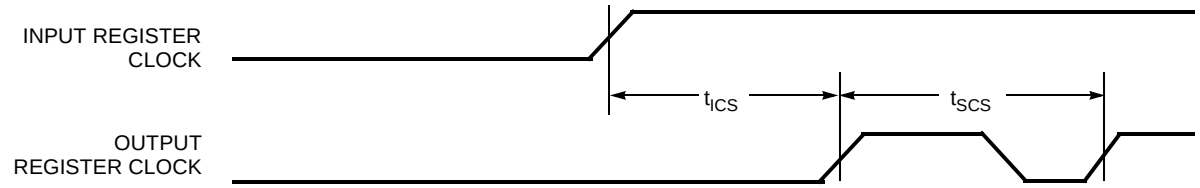


Registered Input

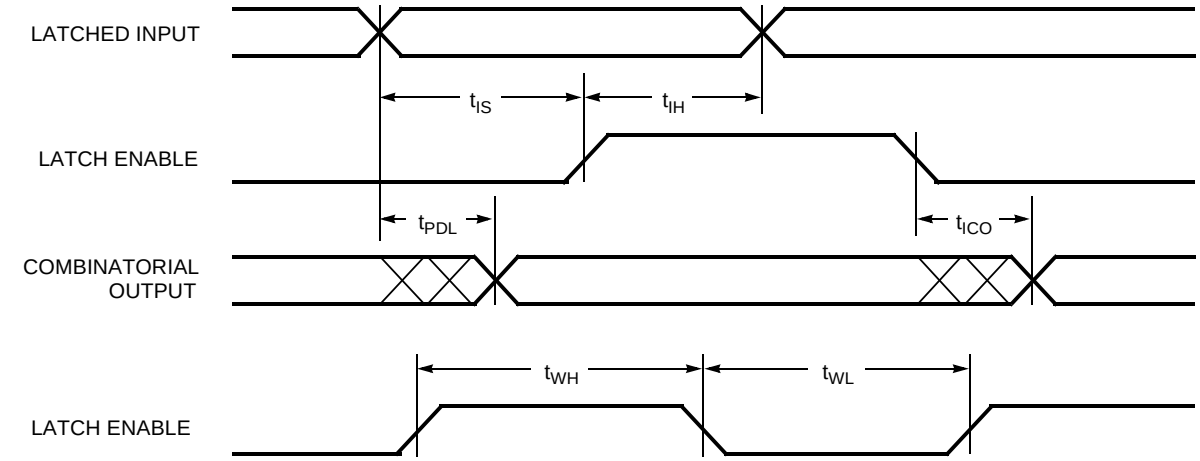


Switching Waveforms (continued)

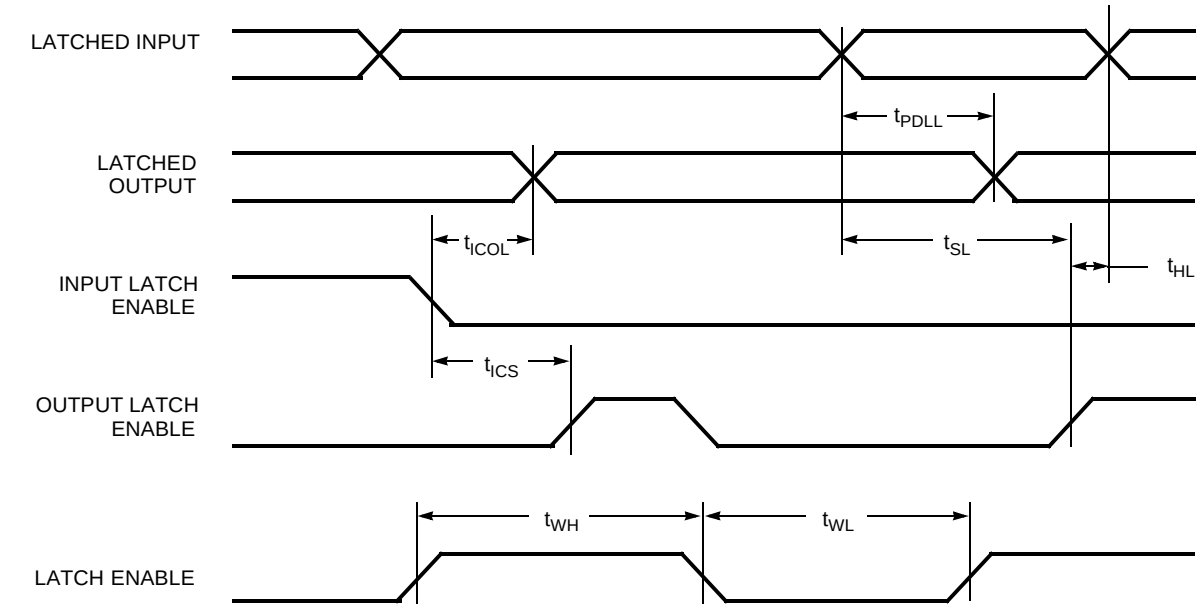
Clock to Clock



Latched Input

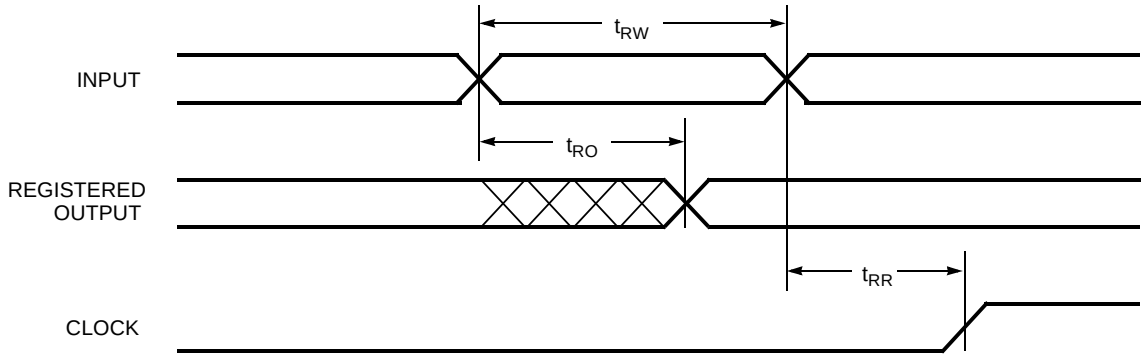


Latched Input and Output

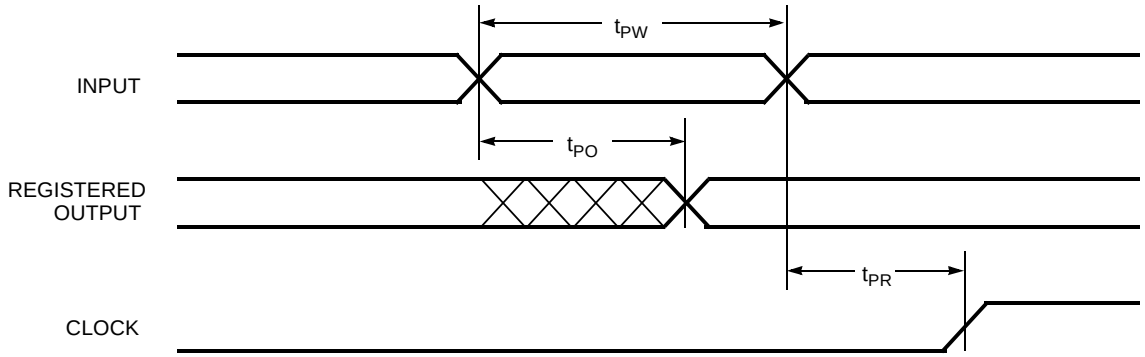


Switching Waveforms (continued)

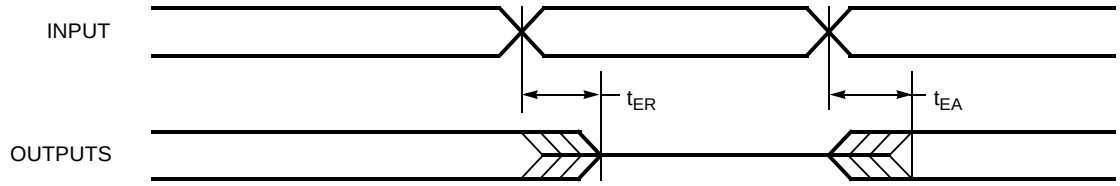
Asynchronous Reset



Asynchronous Preset



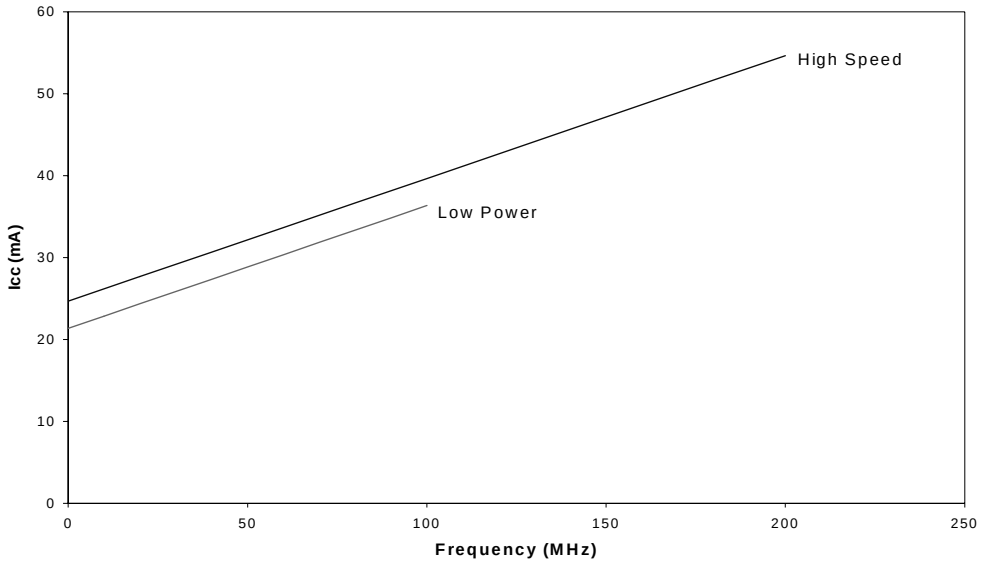
Output Enable/Disable



Power Consumption

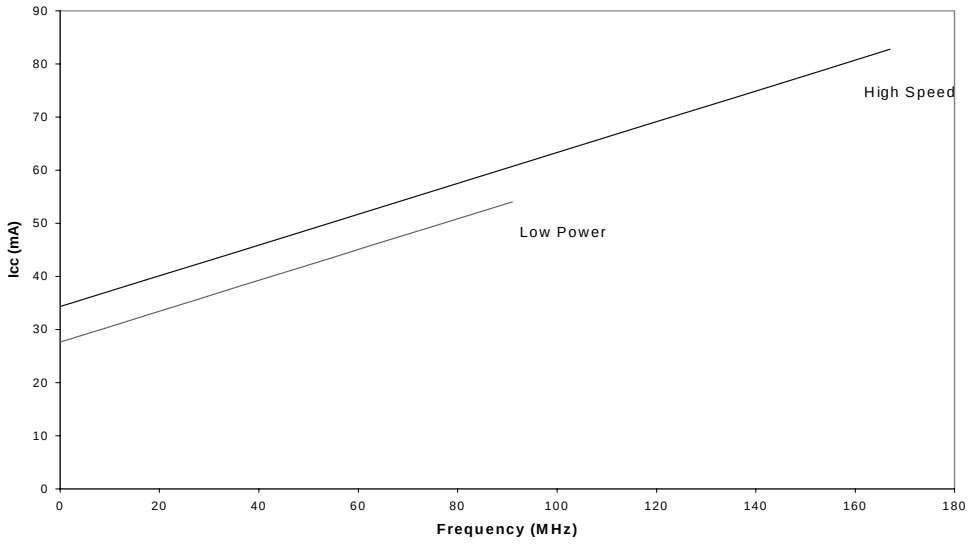
Typical 5.0V Power Consumption

CY37032



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

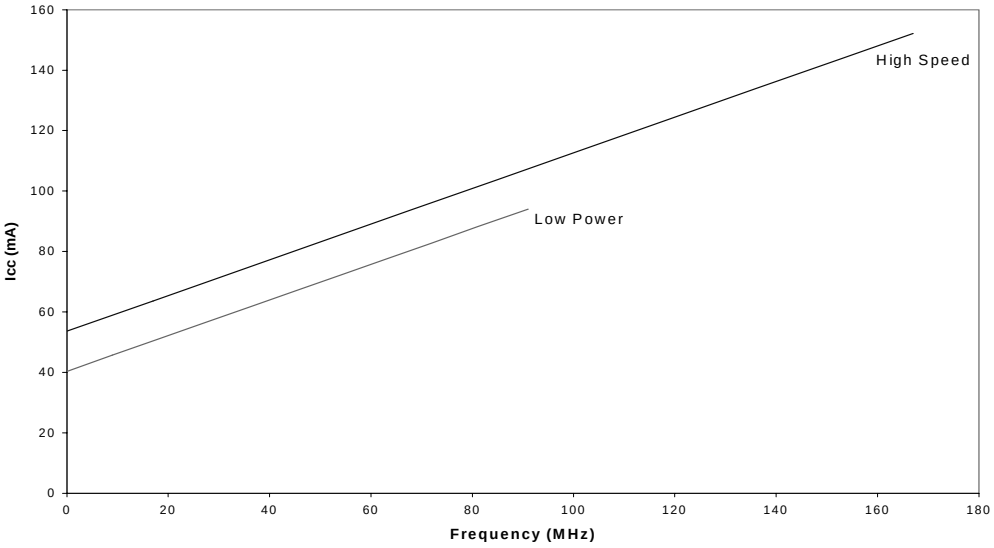
CY37064



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

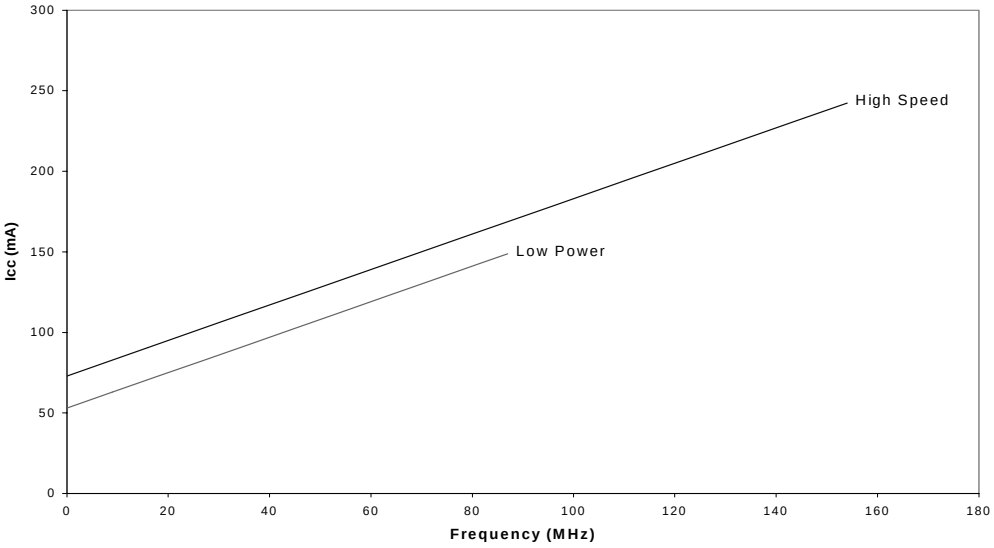
Typical 5.0V Power Consumption (continued)

CY37128



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

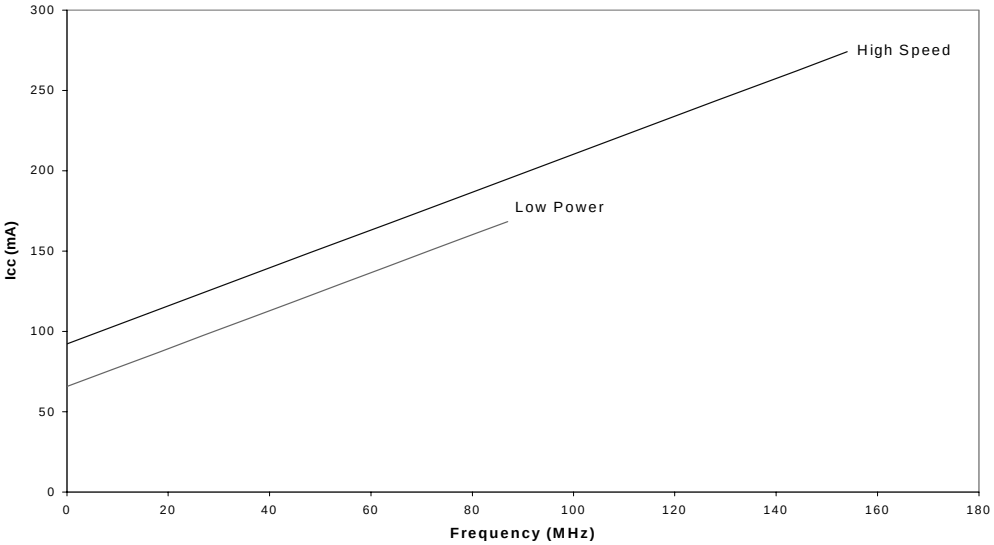
CY37192



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

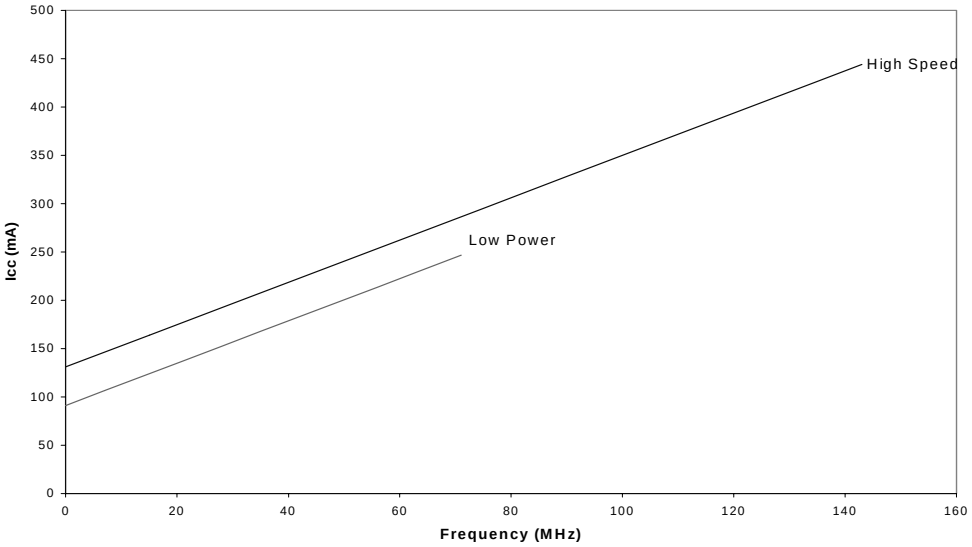
Typical 5.0V Power Consumption (continued)

CY37256



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

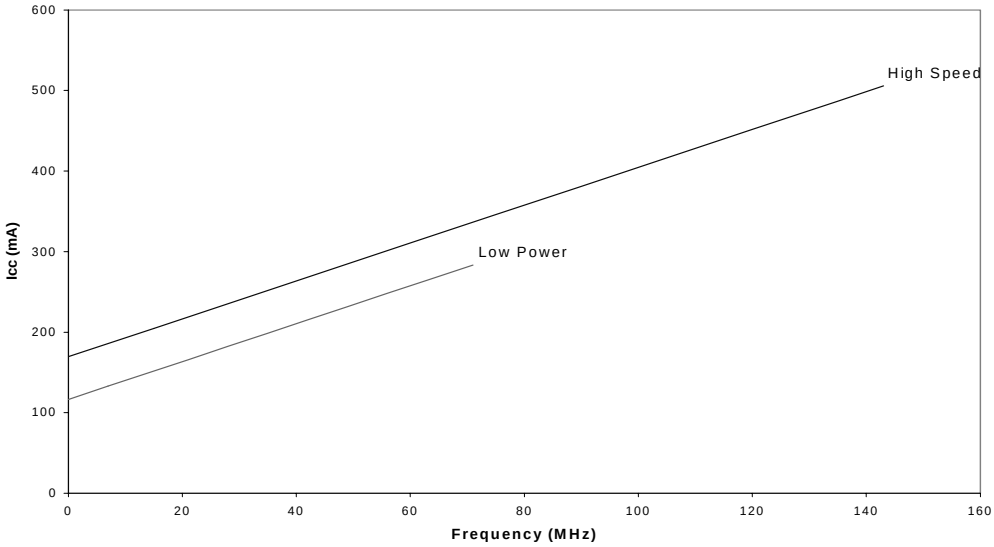
CY37384



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

Typical 5.0V Power Consumption (continued)

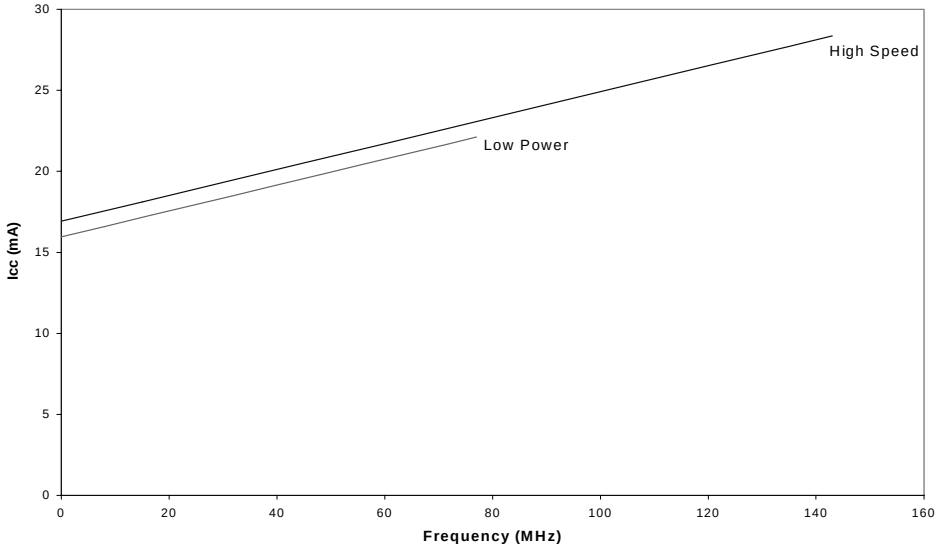
CY37512



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

Typical 3.3V Power Consumption

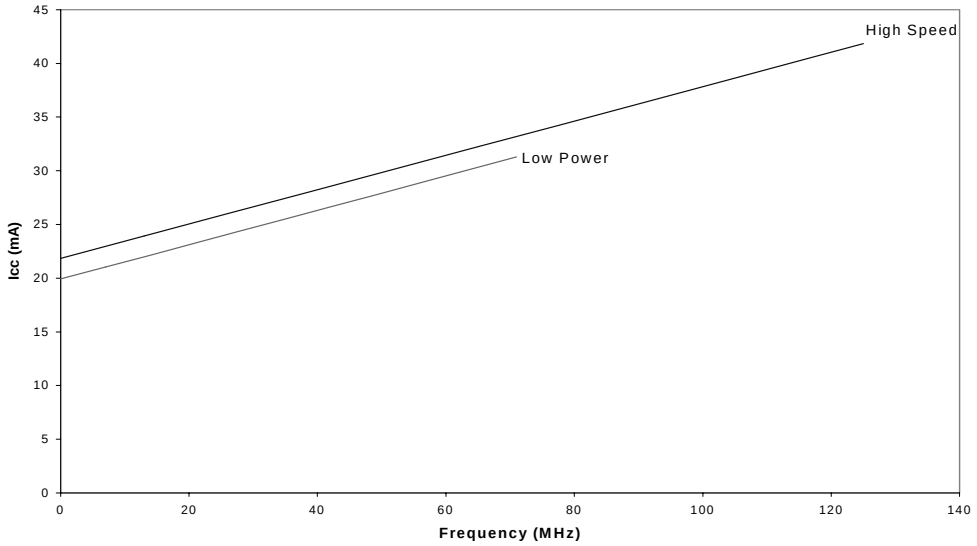
CY37032V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

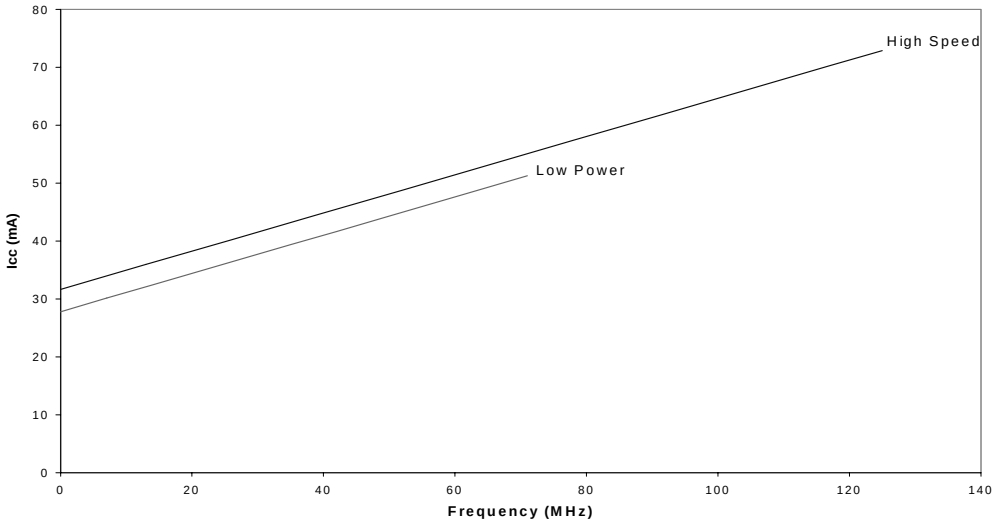
Typical 3.3V Power Consumption (continued)

CY37064V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

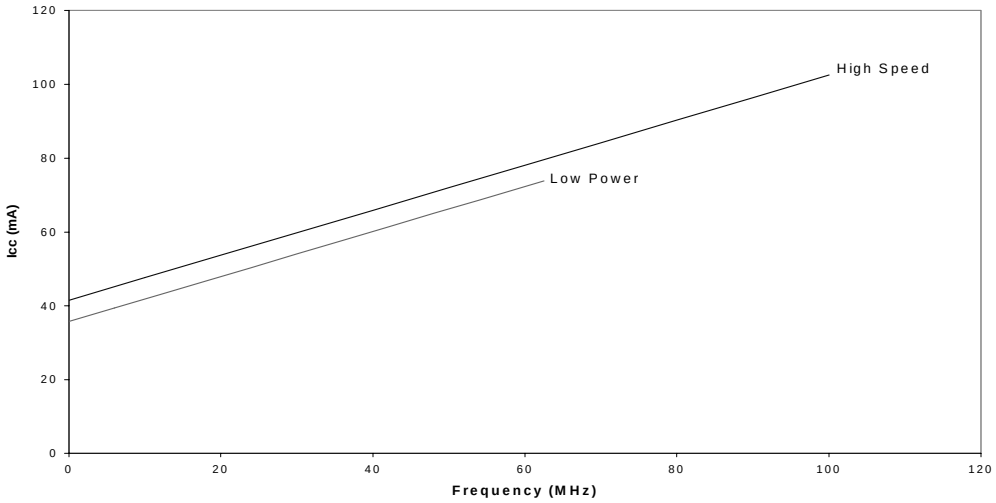
CY37128V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

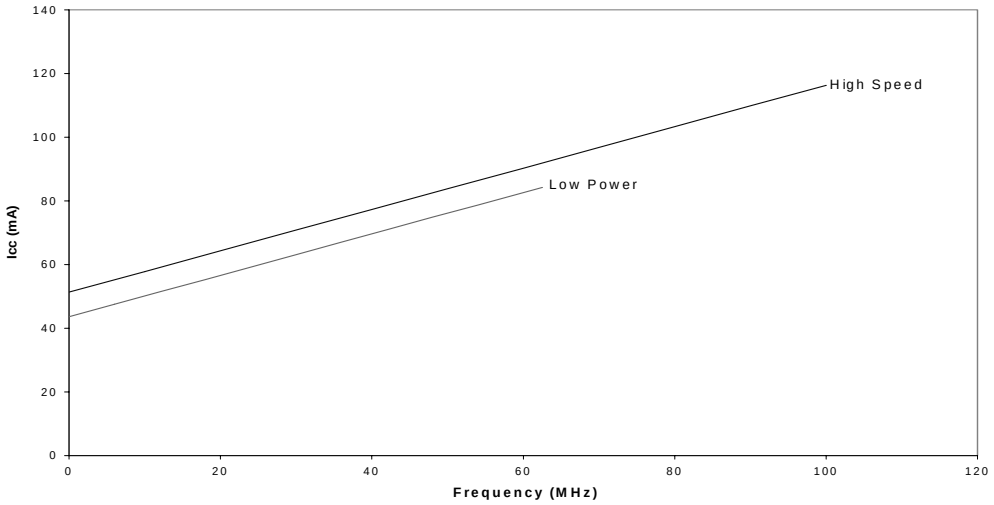
Typical 3.3V Power Consumption (continued)

CY37192V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

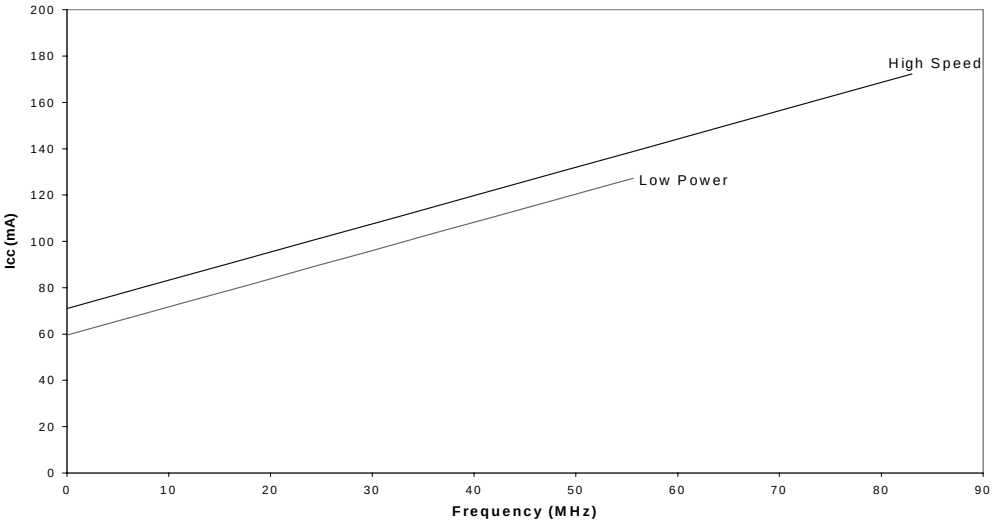
CY37256V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

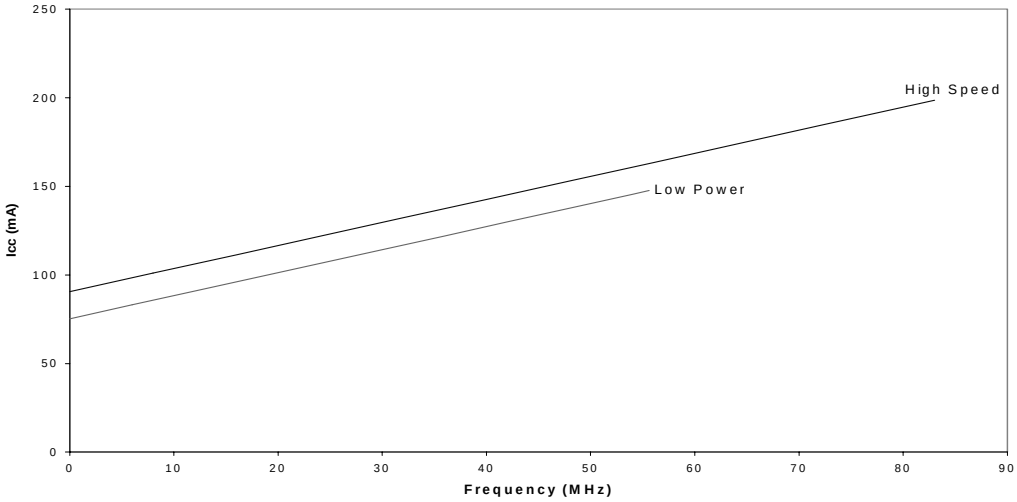
Typical 3.3V Power Consumption (continued)

CY37384V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

CY37512V

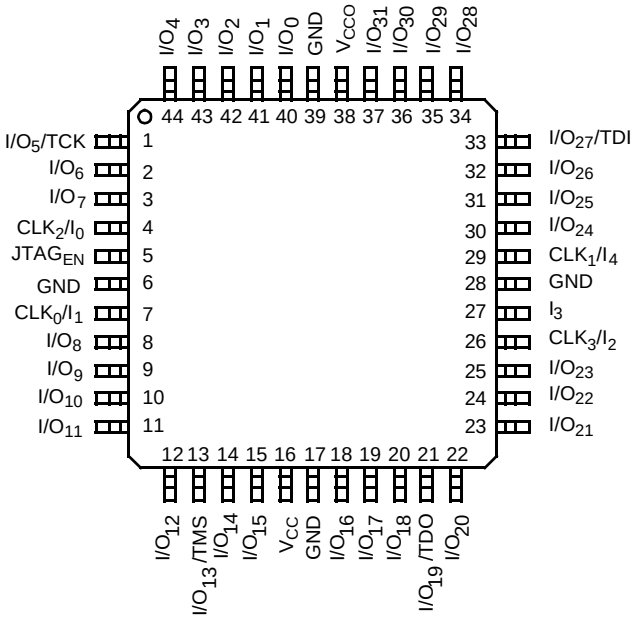


The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

Pin Configurations[19]

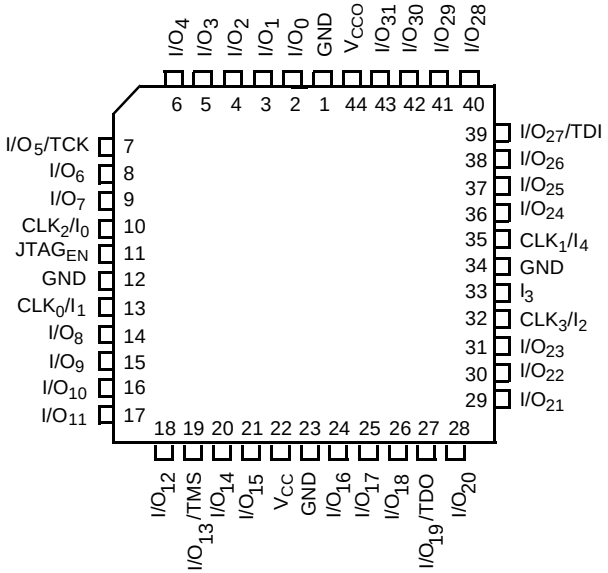
44-Pin TQFP (A44)

Top View



44-Pin PLCC (J67) / CLCC (Y67)

Top View



Note:
19. For 3.3V versions (Ultra37000V), $V_{CCO} = V_{CC}$.

Pin Configurations[19] (continued)

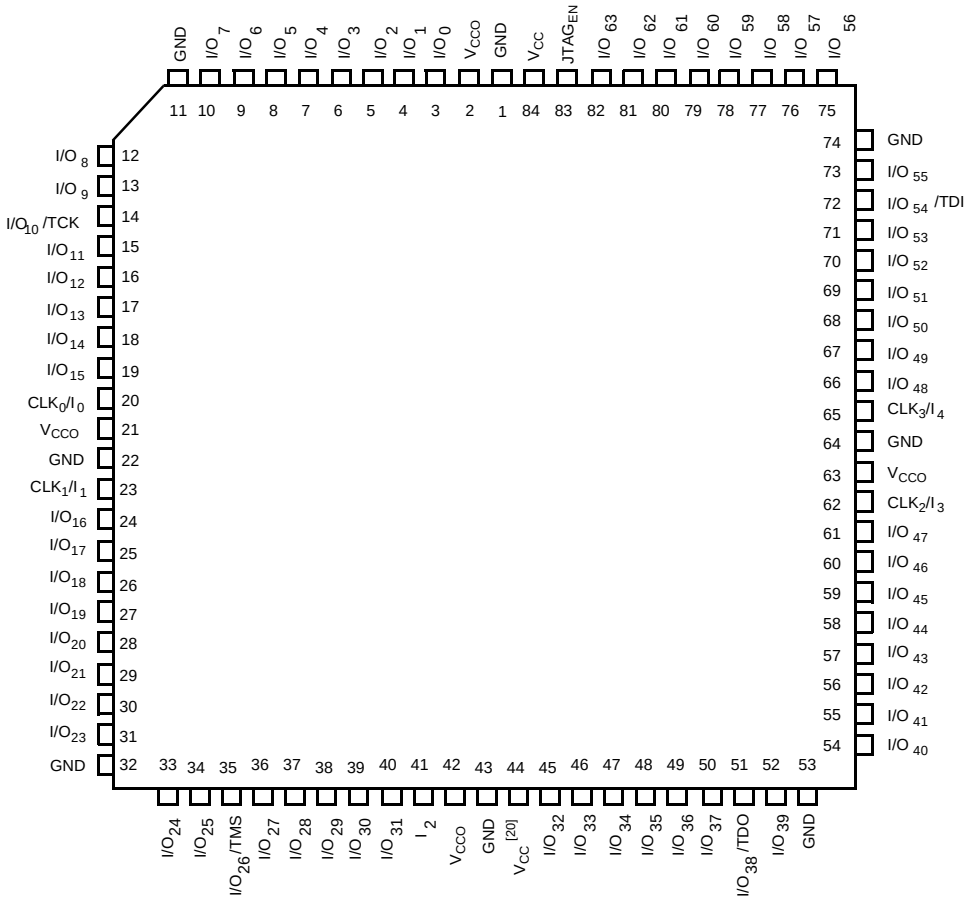
48-Ball Fine-Pitch BGA (BA50)
Top View

	1	2	3	4	5	6	7	8
A	I/O_5 TCK	V_{CC}	I/O_3	I/O_1	I/O_{31}	I/O_{30}	V_{CC}	I/O_{27} TDI
B	V_{CC}	I/O_4	I/O_2	I/O_0	I/O_{29}	I/O_{28}	I/O_{26}	CLK_1/ I_4
C	CLK_2/ I_0	I/O_7	I/O_6	GND	GND	I/O_{25}	I/O_{24}	I_3
D	$JTAG_{EN}$	I/O_8	I/O_9	GND	GND	I/O_{22}	I/O_{23}	CLK_3/ I_2
E	CLK_0/ I_1	I/O_{12}	I/O_{11}	I/O_{10}	I/O_{16}	I/O_{20}	I/O_{21}	V_{CC}
F	I/O_{13} TMS	V_{CC}	I/O_{14}	I/O_{15}	I/O_{17}	I/O_{18}	V_{CC}	I/O_{19} TDO

Pin Configurations[19] (continued)

84-Lead PLCC (J83) / CLCC (Y84)

Top View

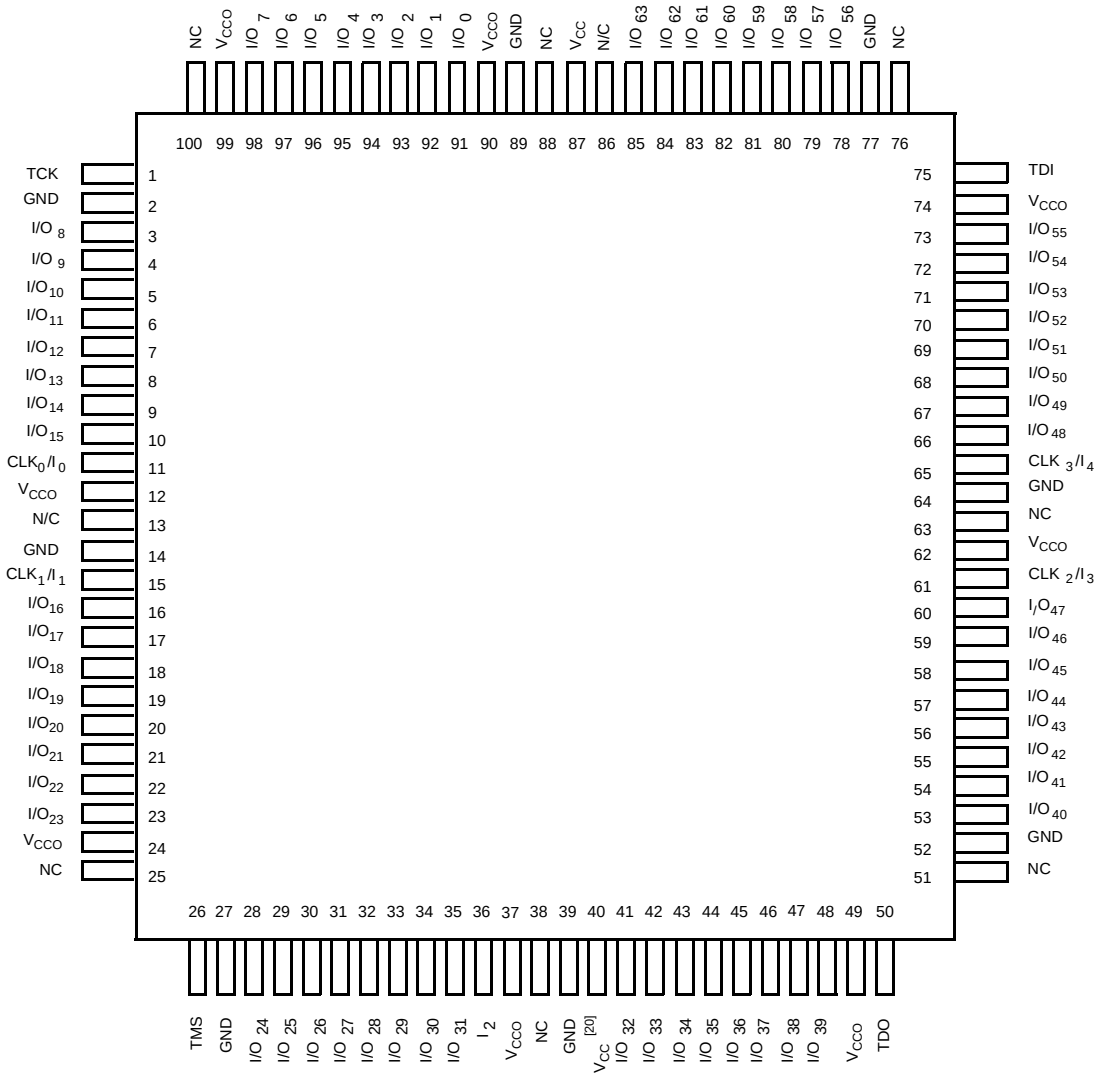


Note:

20. This pin is a N/C, but Cypress recommends that you connect it to V_{CC} to ensure future compatibility.

Pin Configurations[19] (continued)

100-Lead TQFP (A100)
Top View



Pin Configurations[19] (continued)

100-Ball Fine-Pitch BGA (BB100)
for CY37064V
Top View

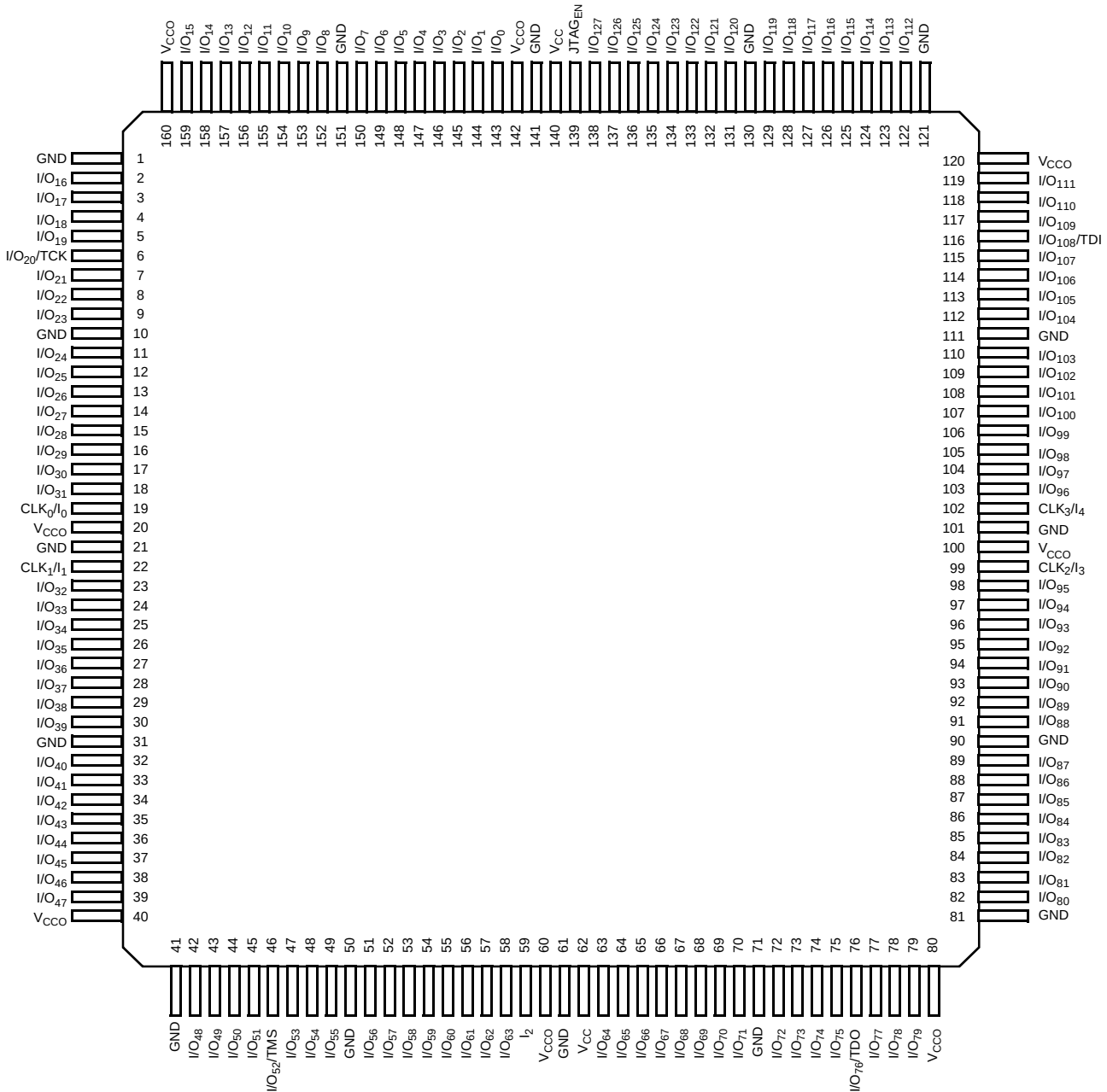
	1	2	3	4	5	6	7	8	9	10
A	NC	NC	I/O_7	I/O_5	I/O_2	I/O_{62}	I/O_{60}	I/O_{58}	I/O_{57}	I/O_{56}
B	I/O_9	I/O_8	I/O_6	I/O_4	I/O_1	I/O_{63}	V_{CC}	I/O_{59}	I/O_{55}	NC
C	I/O_{10}	TCK	V_{CC}	I/O_3	NC	NC	I/O_{61}	V_{CC}	TDI	I/O_{54}
D	I/O_{11}	NC	I/O_{12}	I/O_{13}	I/O_0	NC	I/O_{51}	I/O_{52}	CLK_3/I_4	I/O_{53}
E	I/O_{14}	CLK_0/I_0	I/O_{15}	NC	GND	GND	I/O_{48}	I/O_{49}	CLK_2/I_3	I/O_{50}
F	I/O_{17}	NC	NC	I/O_{16}	GND	GND	NC	NC	I_2	I/O_{47}
G	I/O_{22}	CLK_1/I_1	I/O_{21}	I/O_{19}	I/O_{18}	I/O_{46}	I/O_{45}	I/O_{44}	NC	I/O_{43}
H	I/O_{23}	TMS	V_{CC}	I/O_{20}	NC	I/O_{32}	I/O_{42}	V_{CC}	TDO	I/O_{41}
J	NC	I/O_{26}	I/O_{28}	NC	I/O_{31}	I/O_{33}	I/O_{35}	I/O_{37}	I/O_{39}	I/O_{40}
K	I/O_{24}	I/O_{25}	I/O_{27}	I/O_{29}	I/O_{30}	I/O_{34}	I/O_{36}	I/O_{38}	NC	NC

100-Ball Fine-Pitch BGA (BB100)
for CY37128V
Top View

	1	2	3	4	5	6	7	8	9	10
A	NC	I/O_9	I/O_8	I/O_6	I/O_3	I/O_{76}	I/O_{74}	I/O_{72}	I/O_{71}	I/O_{70}
B	I/O_{11}	I/O_{10}	I/O_7	I/O_5	I/O_2	I/O_{77}	V_{CC}	I/O_{73}	I/O_{68}	I/O_{69}
C	I/O_{12}	I/O_{13} TCK	V_{CC}	I/O_4	I/O_1	I/O_{78}	I/O_{75}	V_{CC}	I/O_{67} TDI	I/O_{66}
D	I/O_{14}	V_{CC}	I/O_{15}	I/O_{16}	I/O_0	I/O_{79}	I/O_{63}	I/O_{64}	CLK_3/I_4	I/O_{65}
E	I/O_{17}	CLK_0/I_0	I/O_{18}	I/O_{19}	GND	GND	I/O_{60}	I/O_{61}	CLK_2/I_3	I/O_{62}
F	I/O_{22}	$JTAG_{EN}$	I/O_{21}	I/O_{20}	GND	GND	I/O_{59}	I/O_{58}	I_2	I/O_{57}
G	I/O_{27}	CLK_1/I_1	I/O_{26}	I/O_{24}	I/O_{23}	I/O_{56}	I/O_{55}	I/O_{54}	V_{CC}	I/O_{53}
H	I/O_{28}	I/O_{33} TMS	V_{CC}	I/O_{25}	I/O_{39}	I/O_{40}	I/O_{52}	V_{CC}	I/O_{47} TDO	I/O_{51}
J	I/O_{29}	I/O_{32}	I/O_{35}	V_{CC}	I/O_{38}	I/O_{41}	I/O_{43}	I/O_{45}	I/O_{48}	I/O_{50}
K	I/O_{30}	I/O_{31}	I/O_{34}	I/O_{36}	I/O_{37}	I/O_{42}	I/O_{44}	I/O_{46}	I/O_{49}	NC

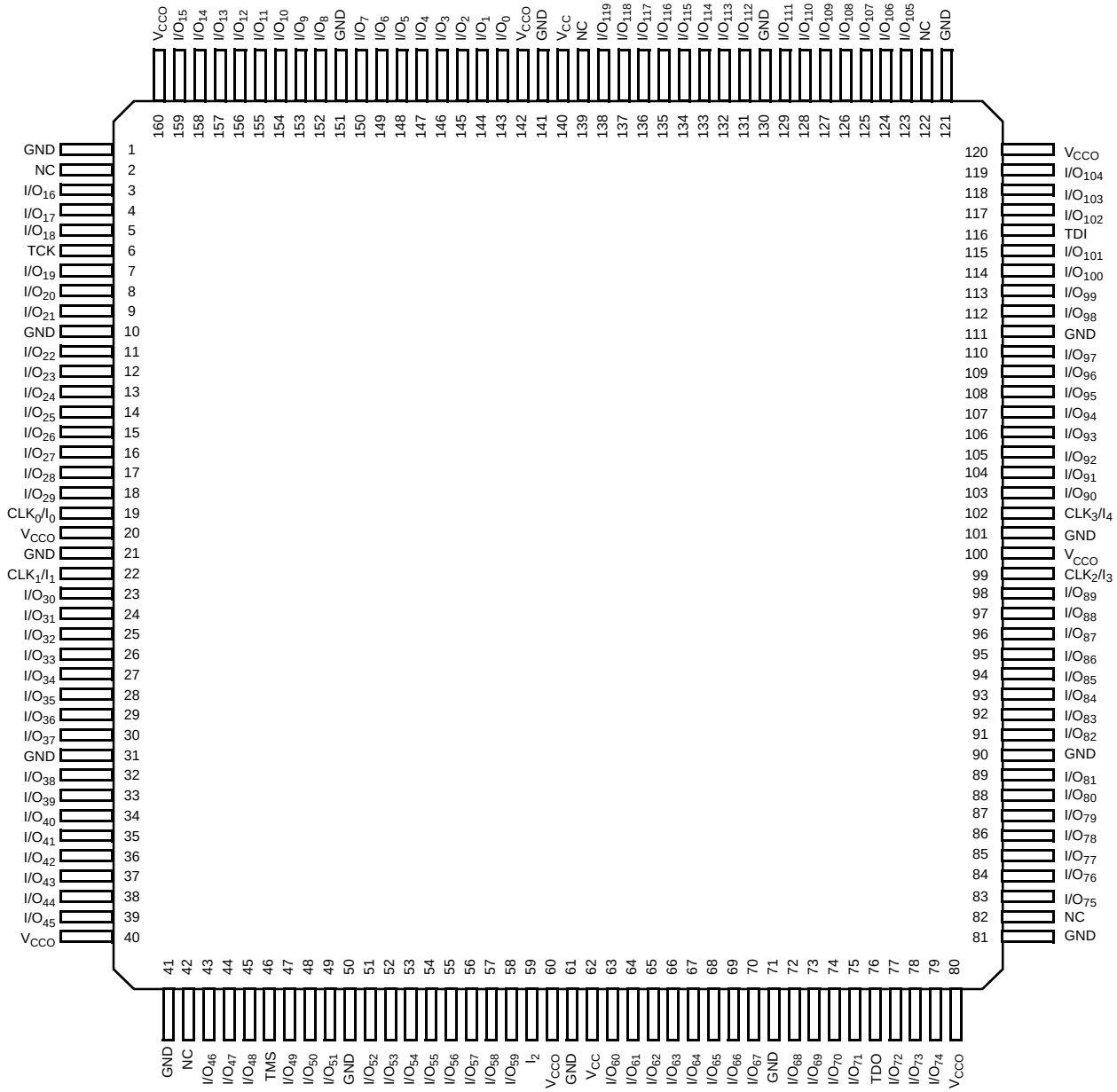
Pin Configurations[19] (continued)

160-Lead TQFP (A160) / CQFP (U162)
for CY37128(V) and CY256(V)
Top View



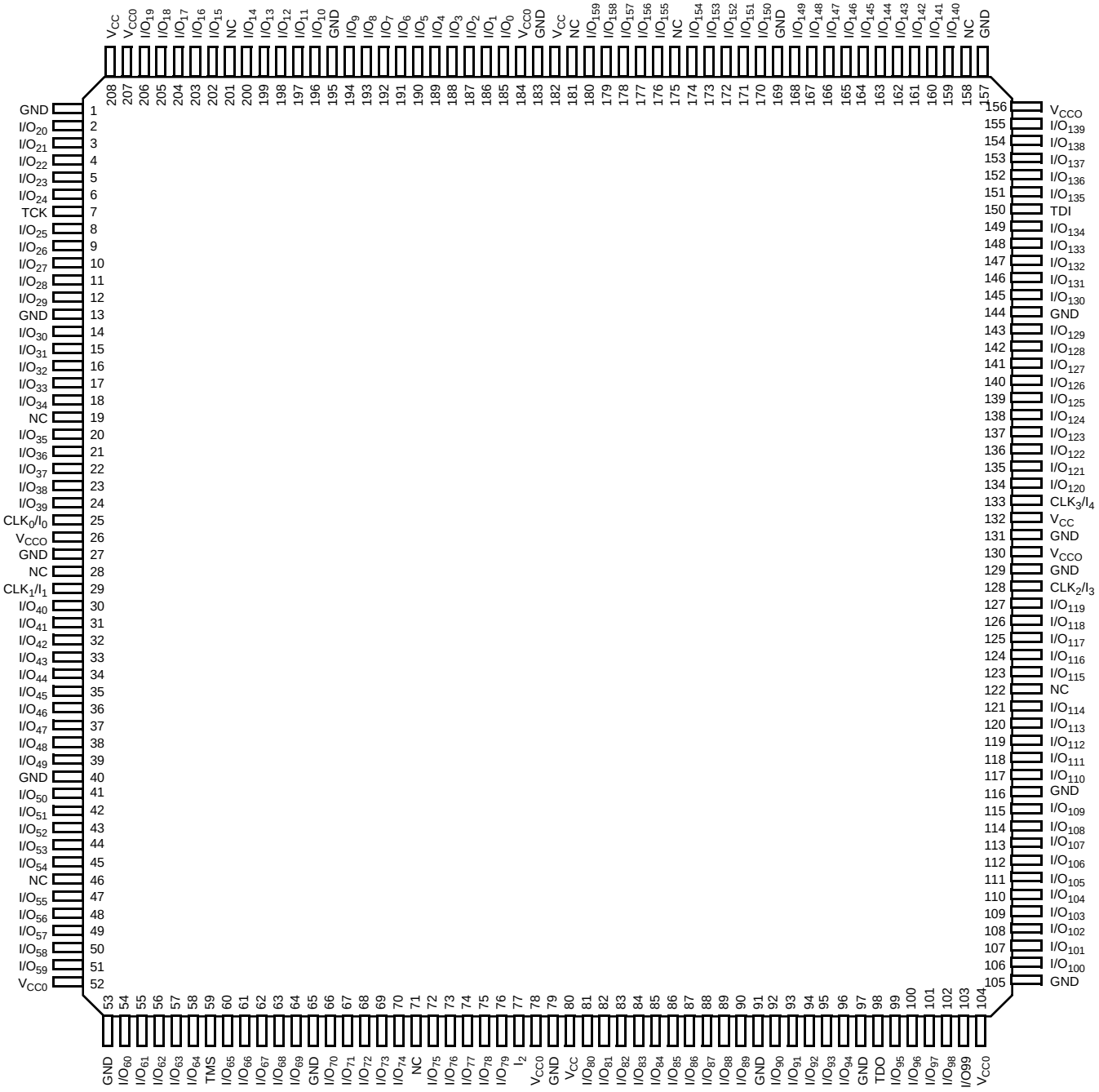
Pin Configurations[19] (continued)

160-Lead TQFP (A160) for CY37192(V)
Top View



Pin Configurations[19] (continued)

208-Lead PQFP (N208) / CQFP (U208)
Top View



Pin Configurations[19] (continued)

256-Ball PBGA (BG256)
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	I/O_{21}	NC	I/O_{16}	I/O_{12}	I/O_{9}	I/O_{7}	I/O_{4}	I/O_{0}	I/O_{190}	I/O_{189}	I/O_{186}	I/O_{182}	NC	I/O_{178}	I/O_{175}	NC	NC	I/O_{169}	I/O_{168}	A
B	I/O_{23}	I/O_{20}	I/O_{19}	I/O_{18}	I/O_{15}	I/O_{11}	I/O_{8}	I/O_{5}	I/O_{1}	I/O_{191}	I/O_{187}	I/O_{185}	I/O_{181}	NC	NC	I/O_{174}	I/O_{171}	I/O_{170}	NC	I/O_{166}	B
C	NC	NC	I/O_{22}	NC	I/O_{17}	I/O_{14}	I/O_{10}	I/O_{6}	I/O_{2}	NC	I/O_{188}	I/O_{184}	I/O_{180}	I/O_{179}	I/O_{176}	I/O_{173}	I/O_{172}	I/O_{167}	I/O_{165}	I/O_{162}	C
D	I/O_{24}	NC	NC	GND	NC	V_{CCO}	I/O_{13}	GND	I/O_{3}	NC	V_{CC}	I/O_{183}	GND	I/O_{177}	V_{CCO}	NC	GND	I/O_{164}	TDI	I/O_{160}	D
E	I/O_{27}	I/O_{26}	I/O_{25}	NC													I/O_{163}	I/O_{161}	I/O_{159}	I/O_{156}	E
F	I/O_{30}	TCK	I/O_{28}	V_{CCO}													V_{CCO}	I/O_{158}	NC	I/O_{154}	F
G	I/O_{33}	I/O_{32}	I/O_{31}	I/O_{29}													I/O_{157}	I/O_{155}	I/O_{153}	I/O_{152}	G
H	I/O_{35}	NC	I/O_{34}	GND				GND	GND	GND	GND	GND	GND				GND	I/O_{151}	I/O_{150}	I/O_{149}	H
J	I/O_{39}	I/O_{38}	I/O_{37}	I/O_{36}				GND	GND	GND	GND	GND	GND				I/O_{148}	I/O_{147}	I/O_{146}	I/O_{145}	J
K	I/O_{42}	I/O_{40}	I/O_{41}	V_{CC}				GND	GND	GND	GND	GND	GND				I/O_{144}	CLK_3/I_4	NC	NC	K
L	I/O_{43}	I/O_{44}	I/O_{45}	I/O_{46}				GND	GND	GND	GND	GND	GND				V_{CC}	CLK_2/I_3	I/O_{143}	NC	L
M	I/O_{47}	CLK_0/I_0	CLK_1/I_1	I/O_{48}				GND	GND	GND	GND	GND	GND				I/O_{139}	I/O_{140}	I/O_{141}	I/O_{142}	M
N	I/O_{49}	I/O_{50}	I/O_{51}	GND				GND	GND	GND	GND	GND	GND				GND	I/O_{136}	I/O_{137}	I/O_{138}	N
P	I/O_{52}	I/O_{53}	I/O_{55}	I/O_{58}													I/O_{131}	I/O_{133}	I/O_{134}	I/O_{135}	P
R	I/O_{54}	I/O_{56}	I/O_{59}	V_{CCO}													V_{CCO}	I/O_{130}	NC	I/O_{132}	R
T	I/O_{57}	I/O_{60}	I/O_{62}	I/O_{65}													I/O_{124}	I/O_{127}	I/O_{128}	I/O_{129}	T
U	I/O_{61}	I/O_{63}	I/O_{66}	GND	I/O_{76}	V_{CCO}	I/O_{82}	GND	I/O_{91}	V_{CC}	I/O_{98}	I/O_{102}	GND	I/O_{112}	V_{CCO}	NC	GND	I/O_{123}	I/O_{122}	I/O_{126}	U
V	I/O_{64}	I/O_{67}	I/O_{69}	I/O_{75}	I/O_{78}	I/O_{81}	I/O_{85}	I/O_{88}	I/O_{92}	I_2	I/O_{97}	I/O_{101}	I/O_{105}	I/O_{109}	I/O_{113}	TDO	I/O_{114}	I/O_{117}	I/O_{121}	I/O_{125}	V
W	I/O_{68}	I/O_{70}	I/O_{72}	I/O_{74}	I/O_{79}	I/O_{83}	I/O_{86}	I/O_{89}	I/O_{93}	I/O_{95}	I/O_{96}	I/O_{100}	I/O_{104}	I/O_{107}	I/O_{110}	NC	NC	I/O_{115}	I/O_{118}	I/O_{120}	W
Y	I/O_{71}	I/O_{73}	I/O_{77}	TMS	I/O_{80}	I/O_{84}	I/O_{87}	I/O_{90}	I/O_{94}	NC	NC	I/O_{99}	I/O_{103}	I/O_{106}	I/O_{108}	I/O_{111}	NC	NC	I/O_{116}	I/O_{119}	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Pin Configurations[19] (continued)

256-Ball Fine-Pitch BGA (BB256)
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	GND	GND	I/O_{26}	I/O_{24}	I/O_{20}	V_{CC}	I/O_{11}	GND	GND	I/O_{186}	V_{CC}	I/O_{177}	I/O_{172}	I/O_{167}	GND	GND
B	GND	I/O_{27}	I/O_{25}	I/O_{23}	I/O_{19}	I/O_{15}	I/O_{10}	GND	GND	I/O_{185}	I/O_{181}	I/O_{176}	I/O_{171}	I/O_{166}	I/O_{165}	GND
C	I/O_{29}	I/O_{28}	NC	I/O_{22}	I/O_{18}	I/O_{14}	I/O_{9}	I/O_{4}	I/O_{191}	I/O_{184}	I/O_{180}	I/O_{175}	I/O_{170}	NC	I/O_{163}	I/O_{164}
D	I/O_{32}	I/O_{31}	I/O_{30}	NC	I/O_{17}	I/O_{13}	I/O_{8}	I/O_{3}	I/O_{190}	I/O_{183}	I/O_{179}	I/O_{174}	I/O_{169}	I/O_{160}	I/O_{161}	I/O_{162}
E	I/O_{35}	I/O_{34}	I/O_{33}	I/O_{21}	I/O_{16}	I/O_{12}	I/O_{7}	I/O_{2}	I/O_{189}	V_{CC}	I/O_{178}	I/O_{173}	I/O_{168}	I/O_{157}	I/O_{158}	I/O_{159}
F	V_{CC}	I/O_{38}	I/O_{37}	I/O_{36}	TCK	V_{CC}	I/O_{6}	I/O_{1}	I/O_{188}	I/O_{182}	V_{CC}	TDI	I/O_{154}	I/O_{155}	I/O_{156}	V_{CC}
G	I/O_{43}	I/O_{42}	I/O_{41}	I/O_{40}	V_{CC}	I/O_{39}	I/O_{5}	I/O_{0}	I/O_{187}	I/O_{148}	I/O_{149}	CLK_3 /I_4	I/O_{150}	I/O_{151}	I/O_{152}	I/O_{153}
H	GND	GND	I/O_{47}	I/O_{46}	CLK_0 /I_0	I/O_{45}	I/O_{44}	GND	GND	I/O_{144}	I/O_{145}	CLK_2 /I_3	I/O_{146}	I/O_{147}	GND	GND
J	GND	GND	I/O_{51}	I/O_{50}	NC	I/O_{49}	I/O_{48}	GND	GND	I/O_{140}	I/O_{141}	I_2	I/O_{142}	I/O_{143}	GND	GND
K	I/O_{57}	I/O_{56}	I/O_{55}	I/O_{54}	CLK_1 /I_1	I/O_{53}	I/O_{52}	I/O_{91}	I/O_{96}	I/O_{101}	I/O_{135}	V_{CC}	I/O_{136}	I/O_{137}	I/O_{138}	I/O_{139}
L	V_{CC}	I/O_{60}	I/O_{59}	I/O_{58}	TMS	V_{CC}	I/O_{86}	I/O_{92}	I/O_{97}	I/O_{102}	V_{CC}	TDO	I/O_{132}	I/O_{133}	I/O_{134}	V_{CC}
M	I/O_{63}	I/O_{62}	I/O_{61}	I/O_{72}	I/O_{77}	I/O_{82}	V_{CC}	I/O_{93}	I/O_{98}	I/O_{103}	I/O_{108}	I/O_{112}	I/O_{117}	I/O_{129}	I/O_{130}	I/O_{131}
N	I/O_{66}	I/O_{65}	I/O_{64}	I/O_{73}	I/O_{78}	I/O_{83}	I/O_{87}	I/O_{94}	I/O_{99}	I/O_{104}	I/O_{109}	I/O_{113}	NC	I/O_{126}	I/O_{127}	I/O_{128}
P	I/O_{68}	I/O_{67}	NC	I/O_{74}	I/O79	I/O_{84}	I/O_{88}	I/O_{95}	I/O_{100}	I/O_{105}	I/O_{110}	I/O_{114}	I/O_{118}	NC	I/O_{124}	I/O_{125}
R	GND	I/O_{69}	I/O_{70}	I/O_{75}	I/O_{80}	I/O_{85}	I/O_{89}	GND	GND	I/O_{106}	I/O_{111}	I/O_{115}	I/O_{119}	I/O_{121}	I/O_{123}	GND
T	GND	GND	I/O_{71}	I/O_{76}	I/O_{81}	V_{CC}	I/O_{90}	GND	GND	I/O_{107}	V_{CC}	I/O_{116}	I/O_{120}	I/O_{122}	GND	GND

Pin Configurations[19] (continued)

352-Lead BGA (BG352)

Top View

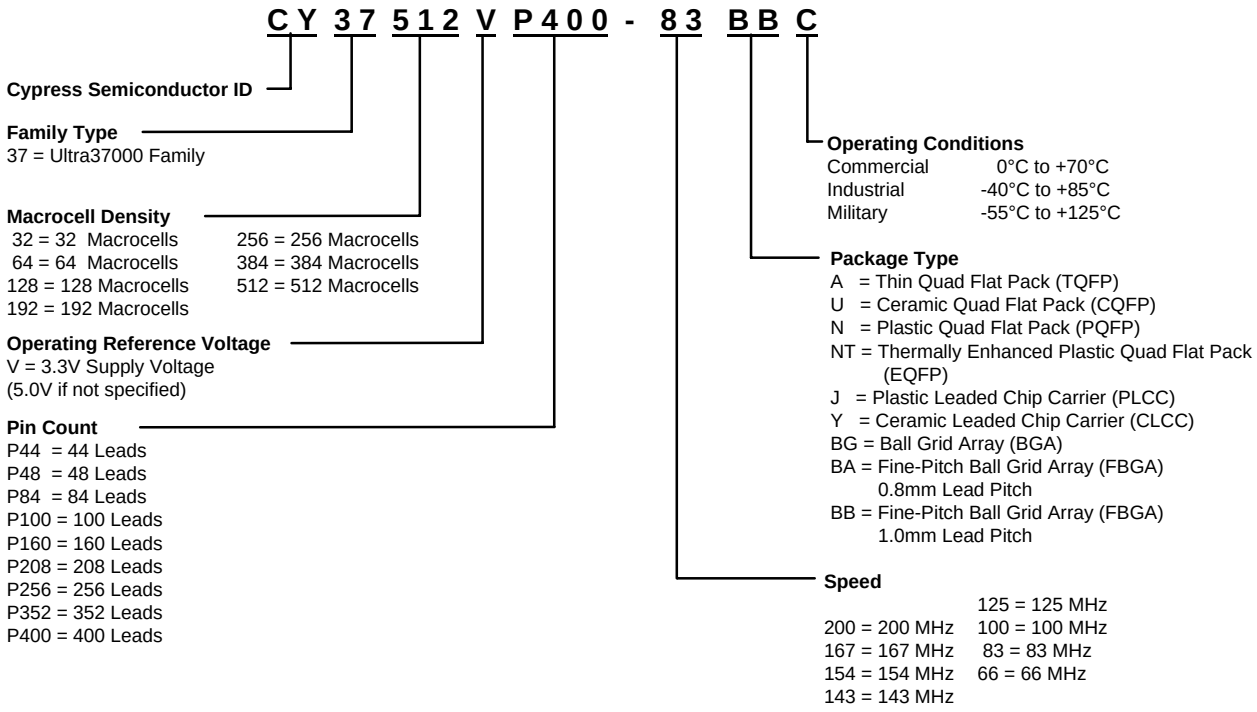
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	GND	GND	I/O_{19}	I/O_{15}	I/O_{13}	I/O_{34}	I/O_{31}	I/O_{28}	I/O_{25}	I/O_{10}	I/O_{7}	I/O_{4}	I/O_{1}	I/O_{263}	I/O_{260}	I/O_{257}	I/O_{254}	I/O_{239}	I/O_{237}	I/O_{232}	I/O_{229}	I/O_{250}	I/O_{248}	I/O_{244}	GND	GND
B	GND	NC	I/O_{18}	I/O_{17}	I/O_{14}	I/O_{35}	I/O_{32}	I/O_{29}	I/O_{26}	I/O_{11}	I/O_{8}	I/O_{5}	I/O_{2}	V_{CC}	I/O_{261}	I/O_{258}	I/O_{255}	I/O_{252}	I/O_{234}	I/O_{231}	I/O_{228}	I/O_{249}	I/O_{246}	I/O_{245}	I/O_{240}	GND
C	I/O_{23}	I/O_{38}	I/O_{37}	I/O_{16}	I/O_{12}	I/O_{33}	I/O_{30}	I/O_{27}	I/O_{24}	I/O_{9}	I/O_{6}	I/O_{3}	I/O_{0}	I/O_{262}	I/O_{259}	I/O_{256}	I/O_{253}	I/O_{238}	I/O_{235}	I/O_{233}	I/O_{230}	I/O_{251}	I/O_{247}	I/O_{225}	I/O_{224}	I/O_{227}
D	I/O_{39}	I/O_{40}	I/O_{36}	NC	NC	I/O_{21}	I/O_{20}	V_{CCO}	V_{CCO}	NC	GND	GND	V_{CCO}	V_{CCO}	GND	GND	NC	V_{CCO}	V_{CCO}	I/O_{236}	I/O_{243}	NC	NC	I/O_{226}	I/O_{222}	I/O_{223}
E	I/O_{42}	TCK	I/O_{41}	NC																			NC	TDI	I/O_{221}	I/O_{220}
F	I/O_{45}	I/O_{44}	I/O_{43}	I/O_{22}																			I/O_{242}	I/O_{219}	I/O_{218}	I/O_{217}
G	I/O_{48}	I/O_{47}	I/O_{46}	I/O_{63}																			I/O_{241}	I/O_{216}	I/O_{215}	I/O_{214}
H	I/O_{49}	I/O_{50}	I/O_{51}	V_{CCO}																			V_{CCO}	I/O_{211}	I/O_{212}	I/O_{213}
J	I/O_{52}	I/O_{53}	I/O_{54}	V_{CCO}																			V_{CCO}	I/O_{208}	I/O_{209}	I/O_{210}
K	I/O_{55}	I/O_{56}	I/O_{57}	NC																			NC	I/O_{205}	I/O_{206}	I/O_{207}
L	I0	I/O_{59}	I/O_{58}	GND							GND	GND	GND	GND	GND	GND							GND	I/O_{204}	I4	I/O_{197}
M	I/O_{61}	I/O_{60}	I1	GND							GND	GND	GND	GND	GND	GND							GND	I3	I/O_{203}	I/O_{202}
N	I/O_{64}	V_{CC}	I/O_{62}	V_{CCO}							GND	GND	GND	GND	GND	GND							V_{CCO}	I/O_{201}	I/O_{200}	I/O_{199}
P	I/O_{65}	I/O_{66}	I/O_{67}	V_{CCO}							GND	GND	GND	GND	GND	GND							V_{CCO}	I/O_{196}	V_{CC}	I/O_{198}
R	I/O_{68}	I/O_{69}	I/O_{70}	GND							GND	GND	GND	GND	GND	GND							GND	I/O_{193}	I/O_{194}	I/O_{195}
T	I/O_{71}	I/O_{84}	I/O_{85}	GND							GND	GND	GND	GND	GND	GND							GND	I/O_{178}	I/O_{179}	I/O_{192}
U	I/O_{88}	I/O_{87}	I/O_{86}	NC																			NC	I/O_{177}	I/O_{176}	I/O_{175}
V	I/O_{91}	I/O_{90}	I/O_{89}	V_{CCO}																			V_{CCO}	I/O_{174}	I/O_{173}	I/O_{172}
W	I/O_{94}	I/O_{93}	I/O_{92}	V_{CCO}																			V_{CCO}	I/O_{171}	I/O_{170}	I/O_{169}
Y	I/O_{95}	I/O_{72}	I/O_{73}	I/O_{110}																			I/O_{153}	I/O_{190}	I/O_{191}	I/O_{168}
AA	I/O_{74}	I/O_{75}	I/O_{76}	I/O_{111}																			I/O_{152}	I/O_{187}	I/O_{188}	I/O_{189}
AB	I/O_{77}	I/O_{78}	I/O_{79}	N/C																			NC	I/O_{184}	I/O_{185}	I/O_{186}
AC	I/O_{81}	I/O_{80}	I/O_{108}	N/C	NC	I/O_{112}	I/O_{113}	V_{CCO}	V_{CCO}	NC	GND	GND	V_{CCO}	V_{CCO}	GND	GND	NC	V_{CCO}	V_{CCO}	I/O_{150}	I/O_{151}	NC	NC	I/O_{155}	I/O_{183}	I/O_{182}
AD	I/O_{109}	I/O_{82}	I/O_{83}	I/O_{117}	I/O_{97}	I/O_{100}	I/O_{102}	I/O_{105}	I/O_{120}	I/O_{123}	I/O_{126}	I/O_{129}	I2	I/O_{133}	I/O_{136}	I/O_{139}	I/O_{142}	I/O_{157}	I/O_{159}	I/O_{161}	I/O_{163}	I/O_{166}	I/O_{146}	I/O_{180}	I/O_{181}	I/O_{154}
AE	GND	NC	I/O_{115}	I/O_{116}	I/O_{119}	I/O_{98}	I/O_{101}	I/O_{103}	I/O_{106}	I/O_{121}	I/O_{124}	I/O_{127}	V_{CC}	I/O_{130}	I/O_{134}	I/O_{137}	I/O_{140}	I/O_{143}	I/O_{160}	I/O_{162}	I/O_{165}	I/O_{144}	I/O_{147}	I/O_{148}	NC	GND
AF	GND	GND	I/O_{114}	I/O_{118}	I/O_{96}	I/O_{99}	TMS	I/O_{104}	I/O_{107}	I/O_{122}	I/O_{125}	I/O_{128}	I/O_{131}	I/O_{132}	I/O_{135}	I/O_{138}	I/O_{141}	I/O_{156}	I/O_{158}	TDO	I/O_{164}	I/O_{167}	I/O_{145}	I/O_{149}	GND	GND

Pin Configurations[19] (continued)

400-Ball Fine-Pitch BGA (BB400)
Top View

A	GND	GND	NC	I/O_{17}	I/O_{16}	I/O_{14}	I/O_{29}	V_{CC}	I/O_{11}	GND	GND	I/O_{257}	V_{CC}	I/O_{239}	I/O_{233}	I/O_{232}	I/O_{230}	NC	GND	GND
B	GND	GND	GND	NC	I/O_{15}	I/O_{13}	I/O_{28}	V_{CC}	I/O_{10}	GND	GND	I/O_{256}	V_{CC}	I/O_{238}	I/O_{231}	I/O_{229}	NC	GND	GND	GND
C	NC	GND	GND	GND	I/O_{20}	I/O_{12}	I/O_{27}	V_{CC}	I/O_{9}	GND	GND	I/O_{255}	V_{CC}	I/O_{237}	I/O_{228}	I/O_{245}	GND	GND	GND	NC
D	I/O_{44}	NC	GND	I/O_{21}	I/O_{19}	I/O_{18}	I/O_{26}	I/O_{25}	I/O_{8}	GND	GND	I/O_{254}	I/O_{235}	I/O_{236}	I/O_{251}	I/O_{244}	I/O_{243}	GND	NC	I/O_{227}
E	I/O_{46}	I/O_{43}	I/O_{23}	I/O_{22}	NC	I/O_{35}	I/O_{34}	I/O_{24}	I/O_{7}	I/O_{4}	I/O_{263}	I/O_{253}	I/O_{234}	I/O_{250}	I/O_{248}	NC	I/O_{241}	I/O_{242}	I/O_{225}	I/O_{226}
F	I/O_{47}	I/O_{45}	I/O_{42}	I/O_{41}	I/O_{40}	NC	I/O_{33}	I/O_{32}	I/O_{6}	I/O_{3}	I/O_{262}	I/O_{252}	I/O_{249}	I/O_{247}	I/O_{220}	I/O_{221}	I/O_{240}	I/O_{222}	I/O_{223}	I/O_{224}
G	I/O_{53}	I/O_{52}	I/O_{51}	I/O_{50}	I/O_{39}	I/O_{38}	I/O_{37}	I/O_{31}	I/O_{5}	I/O_{2}	I/O_{261}	V_{CC}	I/O_{246}	I/O_{217}	I/O_{218}	I/O_{219}	I/O_{212}	I/O_{213}	I/O_{214}	I/O_{215}
H	V_{CC}	V_{CC}	V_{CC}	I/O_{49}	I/O_{48}	I/O_{36}	TCK	V_{CC}	I/O_{30}	I/O_{1}	I/O_{259}	I/O_{260}	V_{CC}	TDI	I/O_{216}	I/O_{210}	I/O_{211}	V_{CC}	V_{CC}	V_{CC}
J	I/O_{59}	I/O_{58}	I/O_{57}	I/O_{56}	I/O_{55}	I/O_{54}	V_{CC}	I/O_{62}	I/O_{60}	I/O_{0}	I/O_{258}	I/O_{202}	I/O_{203}	CLK_3 /I_4	I/O_{204}	I/O_{205}	I/O_{206}	I/O_{207}	I/O_{208}	I/O_{209}
K	GND	GND	GND	GND	I/O_{65}	I/O_{64}	CLK_0 /I_0	I/O_{63}	I/O_{61}	GND	GND	I/O_{198}	I/O_{199}	CLK_2 /I_3	I/O_{200}	I/O_{201}	GND	GND	GND	GND
L	GND	GND	GND	GND	I/O_{69}	I/O_{68}	NC	I/O_{67}	I/O_{66}	GND	GND	I/O_{193}	I/O_{195}	I_2	I/O_{196}	I/O_{197}	GND	GND	GND	GND
M	I/O_{89}	I/O_{88}	I/O_{87}	I/O_{86}	I/O_{85}	I/O_{84}	CLK_1 /I_1	I/O_{71}	I/O_{70}	I/O_{126}	I/O_{132}	I/O_{192}	I/O_{194}	V_{CC}	I/O_{174}	I/O_{175}	I/O_{176}	I/O_{177}	I/O_{178}	I/O_{179}
N	V_{CC}	V_{CC}	V_{CC}	I/O_{91}	I/O_{90}	I/O_{72}	TMS	V_{CC}	I/O_{128}	I/O_{127}	I/O_{133}	I/O_{162}	V_{CC}	TDO	I/O_{180}	I/O_{168}	I/O_{169}	V_{CC}	V_{CC}	V_{CC}
P	I/O_{95}	I/O_{94}	I/O_{93}	I/O_{92}	I/O_{75}	I/O_{74}	I/O_{73}	I/O_{114}	V_{CC}	I/O_{129}	I/O_{134}	I/O_{137}	I/O_{163}	I/O_{181}	I/O_{182}	I/O_{183}	I/O_{170}	I/O_{171}	I/O_{172}	I/O_{173}
R	I/O_{80}	I/O_{79}	I/O_{78}	I/O_{108}	I/O_{77}	I/O_{76}	I/O_{115}	I/O_{117}	I/O_{120}	I/O_{130}	I/O_{135}	I/O_{138}	I/O_{164}	I/O_{165}	NC	I/O_{184}	I/O_{185}	I/O_{186}	I/O_{189}	I/O_{191}
T	I/O_{82}	I/O_{81}	I/O_{110}	I/O_{109}	NC	I/O_{116}	I/O_{118}	I/O_{102}	I/O_{121}	I/O_{131}	I/O_{136}	I/O_{139}	I/O_{156}	I/O_{166}	I/O_{167}	NC	I/O_{154}	I/O_{155}	I/O_{187}	I/O_{190}
U	I/O_{83}	NC	GND	I/O_{111}	I/O_{112}	I/O_{119}	I/O_{104}	I/O_{103}	I/O_{122}	GND	GND	I/O_{140}	I/O_{157}	I/O_{158}	I/O_{150}	I/O_{151}	I/O_{153}	GND	NC	I/O_{188}
V	NC	GND	GND	GND	I/O_{113}	I/O_{96}	I/O_{105}	V_{CC}	I/O_{123}	GND	GND	I/O_{141}	V_{CC}	I/O_{159}	I/O144	I/O_{152}	GND	GND	GND	NC
W	GND	GND	GND	NC	I/O_{97}	I/O_{99}	I/O_{106}	V_{CC}	I/O_{124}	GND	GND	I/O_{142}	V_{CC}	I/O_{160}	I/O_{145}	I/O_{147}	NC	GND	GND	GND
Y	GND	GND	NC	I/O_{98}	I/O_{100}	I/O_{101}	I/O_{107}	V_{CC}	I/O_{125}	GND	GND	I/O_{143}	V_{CC}	I/O_{161}	I/O_{146}	I/O_{148}	I/O_{149}	NC	GND	GND

Ordering Information



5.0V Ordering Information

Macro-cells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
32	200	CY37032P44-200AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032P44-200JC	J67	44-Lead Plastic Leaded Chip Carrier	
	154	CY37032P44-154AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032P44-154JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-154AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032P44-154JI	J67	44-Lead Plastic Leaded Chip Carrier	
	125	CY37032P44-125AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032P44-125JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-125AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032P44-125JI	J67	44-Lead Plastic Leaded Chip Carrier	

5.0V Ordering Information (continued)

Macro-cells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
64	200	CY37064P44-200AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-200JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-200JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-200AC	A100	100-Lead Thin Quad Flat Pack	
	154	CY37064P44-154AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-154JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-154JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-154AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P44-154AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37064P44-154JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-154JI	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-154AI	A100	100-Lead Thin Quad Flat Pack	
		5962-9951902QYA	Y67	44-Lead Ceramic Leadless Chip Carrier	Military
	125	CY37064P44-125AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-125JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-125JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-125AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P44-125AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37064P44-125JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-125JI	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-125AI	A100	100-Lead Thin Quad Flat Pack	
		5962-9951901QYA	Y67	44-Lead Ceramic Leadless Chip Carrier	Military
128	167	CY37128P84-167JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128P100-167AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128P160-167AC	A160	160-Lead Thin Quad Flat Pack	
	125	CY37128P84-125JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128P100-125AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128P160-125AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128P84-125JI	J83	84-Lead Plastic Leaded Chip Carrier	Industrial
		CY37128P100-125AI	A100	100-Lead Thin Quad Flat Pack	
		CY37128P160-125AI	A160	160-Lead Thin Quad Flat Pack	
		5962-9952102QYA	Y84	84-Lead Ceramic Leaded Chip Carrier	Military
	100	CY37128P84-100JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128P100-100AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128P160-100AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128P84-100JI	J83	84-Lead Plastic Leaded Chip Carrier	Industrial
		CY37128P100-100AI	A100	100-Lead Thin Quad Flat Pack	
		CY37128P160-100AI	A160	160-Lead Thin Quad Flat Pack	
		5962-9952101QYA	Y84	84-Lead Ceramic Leaded Chip Carrier	Military

5.0V Ordering Information (continued)

Macro-cells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
192	154	CY37192P160-154AC	A160	160-Lead Thin Quad Flat Pack	Commercial
	125	CY37192P160-125AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192P160-125AI	A160	160-Lead Thin Quad Flat Pack	Industrial
	83	CY37192P160-83AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192P160-83AI	A160	160-Lead Thin Quad Flat Pack	Industrial
256	154	CY37256P160-154AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P208-154NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-154BGC	BG256	256-Lead Ball Grid Array	
	125	CY37256P160-125AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P208-125NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-125BGC	BG256	256-Lead Ball Grid Array	
		CY37256P160-125AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256P208-125NI	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-125BGI	BG256	256-Lead Ball Grid Array	
		5962-9952302QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
	83	CY37256P160-83AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P208-83NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-83BGC	BG256	256-Lead Ball Grid Array	
		CY37256P160-83AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256P208-83NI	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-83BGI	BG256	256-Lead Ball Grid Array	
		5962-9952301QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
384	125	CY37384P208-125NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384P256-125BGC	BG256	256-Lead Ball Grid Array	
	83	CY37384P208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384P256-83BGC	BG256	256-Lead Ball Grid Array	
		CY37384P208-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37384P256-83BGI	BG256	256-Lead Ball Grid Array	

5.0V Ordering Information (continued)

Macro-cells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
512	125	CY37512P208-125NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-125BGC	BG256	256-Lead Ball Grid Array	
		CY37512P352-125BGC	BG352	352-Lead Ball Grid Array	
	100	CY37512P208-100NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-100BGC	BG256	256-Lead Ball Grid Array	
		CY37512P352-100BGC	BG352	352-Lead Ball Grid Array	
		CY37512P208-100NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512P256-100BGI	BG256	256-Lead Ball Grid Array	
		CY37512P352-100BGI	BG352	352-Lead Ball Grid Array	
		5962-9952502QZC	U208	208-Lead Ceramic Quad Flat Pack	Military
	83	CY37512P208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-83BGC	BG256	256-Lead Ball Grid Array	
		CY37512P352-83BGC	BG352	352-Lead Ball Grid Array	
		CY37512P208-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512P256-83BGI	BG256	256-Lead Ball Grid Array	
		CY37512P352-83BGI	BG352	352-Lead Ball Grid Array	
		5962-9952501QZC	U208	208-Lead Ceramic Quad Flat Pack	Military

3.3V Ordering Information

Macro-cells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
32	143	CY37032VP44-143AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032VP44-143JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032VP48-143BAC	BA50	48-Lead Fine Pitch Ball Grid Array	
	100	CY37032VP44-100AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032VP44-100JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032VP48-100BAC	BA50	48-Lead Fine Pitch Ball Grid Array	
		CY37032VP44-100AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032VP44-100JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032VP48-100BAI	BA50	48-Lead Fine Pitch Ball Grid Array	

3.3V Ordering Information (continued)

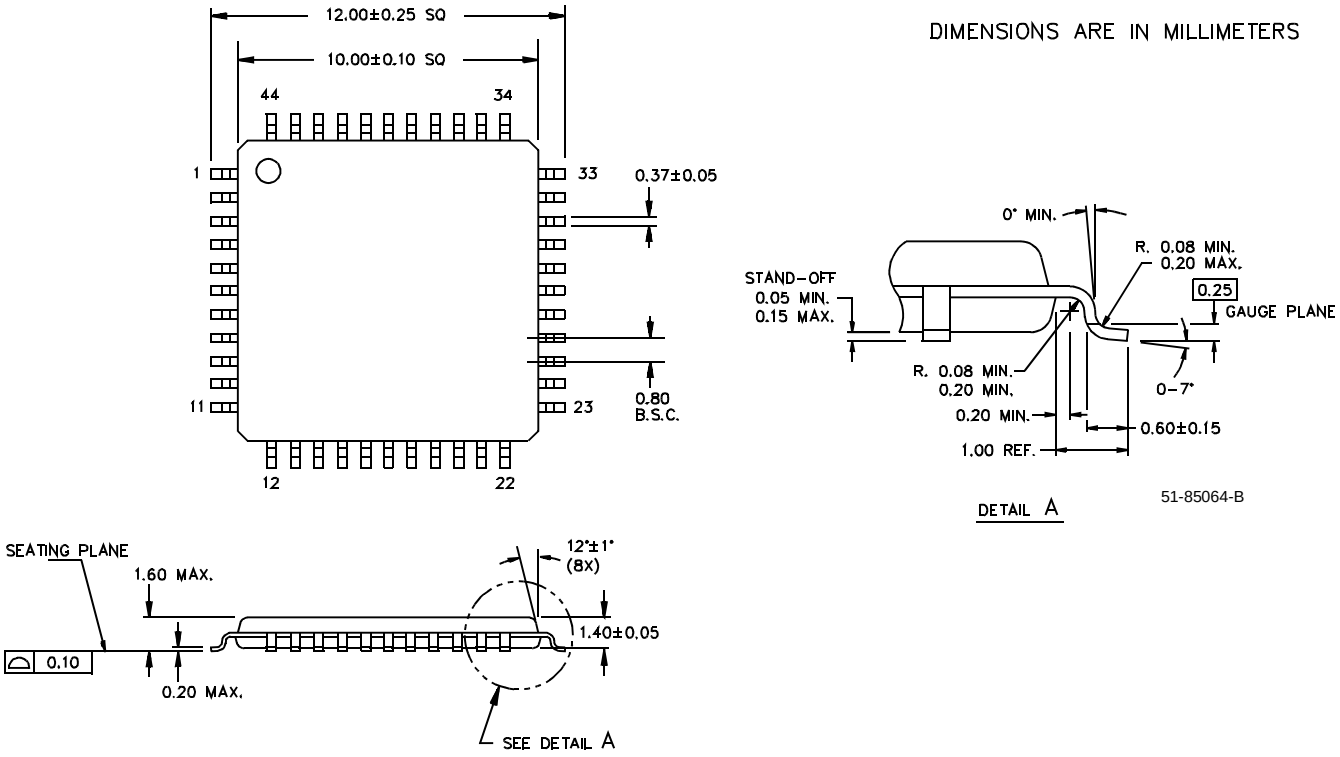
Macro-cells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
64	143	CY37064VP44-143AC	A44	44-Lead Thin Quad Flatpack	Commercial
		CY37064VP44-143JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064VP48-143BAC	BA50	48-Lead Fine-Pitch Ball Grid Array	
		CY37064VP84-143JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064VP100-143AC	A100	100-Lead Thin Quad Flatpack	
		CY37064VP100-143BBC	BB100	100-Lead Fine-Pitch Ball Grid Array	
	100	CY37064VP44-100AC	A44	44-Lead Thin Quad Flatpack	Commercial
		CY37064VP44-100JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064VP48-100BAC	BA50	48-Lead Fine-Pitch Ball Grid Array	
		CY37064VP84-100JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064VP100-100AC	A100	100-Lead Thin Quad Flatpack	
		CY37064VP100-100BBC	BB100	100-Lead Fine-Pitch Ball Grid Array	
		CY37064VP44-100AI	A44	44-Lead Thin Quad Flatpack	Industrial
		CY37064VP44-100JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064VP48-100BAI	BA50	48-Lead Fine-Pitch Ball Grid Array	
		CY37064VP84-100JI	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064VP100-100BBI	BB100	100-Lead Fine-Pitch Ball Grid Array	
		CY37064VP100-100AI	A100	100-Lead Thin Quad Flatpack	
		5962-9952001QYA	Y67	44-Lead Ceramic Leaded Chip Carrier	Military
128	125	CY37128VP84-125JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128VP100-125AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128VP100-125BBC	BB100	100-Lead Fine-Pitch Ball Grid Array	
		CY37128VP160-125AC	A160	160-Lead Thin Quad Flat Pack	
	83	CY37128VP84-83JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128VP100-83AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128VP100-83BBC	BB100	100-Lead Fine-Pitch Ball Grid Array	
		CY37128VP160-83AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128VP84-83JI	J83	84-Lead Plastic Leaded Chip Carrier	Industrial
		CY37128VP100-83AI	A100	100-Lead Thin Quad Flat Pack	
		CY37128VP100-83BBI	BB100	100-Lead Fine-Pitch Ball Grid Array	
		CY37128VP160-83AI	A160	160-Lead Thin Quad Flat Pack	
		5962-9952201QYA	Y84	84-Lead Ceramic Leaded Chip Carrier	Military
192	100	CY37192VP160-100AC	A160	160-Lead Thin Quad Flat Pack	Commercial
	66	CY37192VP160-66AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192VP160-66AI	A160	160-Lead Thin Quad Flat Pack	Industrial

3.3V Ordering Information (continued)

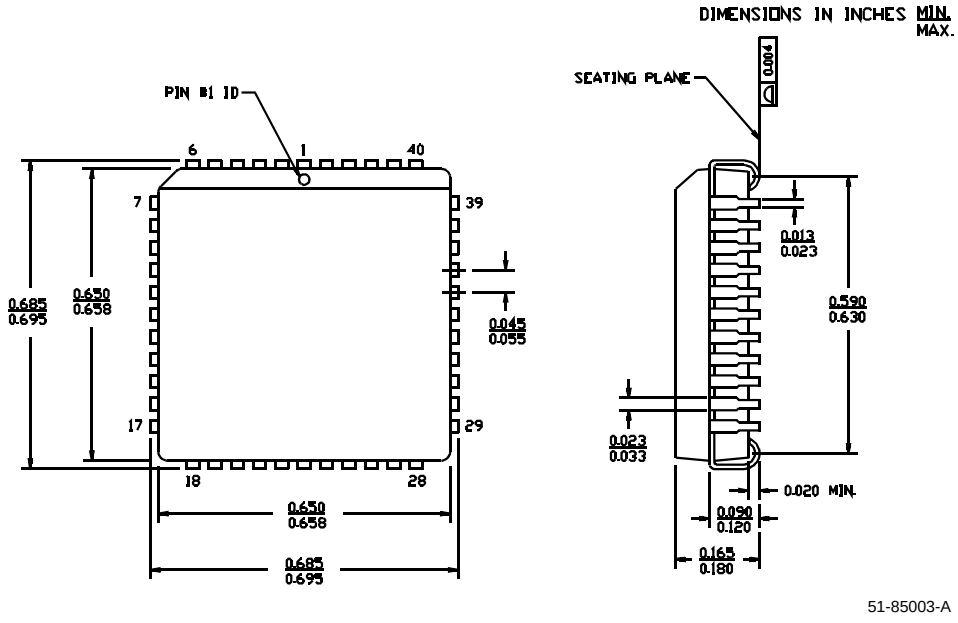
Macro-cells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
256	100	CY37256VP160-100AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP208-100NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-100BGC	BG256	256-Lead Ball Grid Array	
		CY37256VP256-100BBC	BB256	256-Lead Fine-Pitch Ball Grid Array	
	66	CY37256VP160-66AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-66BGC	BG256	256-Lead Ball Grid Array	
		CY37256VP256-66BBC	BB256	256-Lead Fine-Pitch Ball Grid Array	
		CY37256VP160-66AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256VP256-66BGI	BG256	256-Lead Ball Grid Array	
		CY37256VP256-66BBI	BB256	256-Lead Fine-Pitch Ball Grid Array	
		5962-9952401QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
384	83	CY37384VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-83BGC	BG256	256-Lead Ball Grid Array	
	66	CY37384VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-66BGC	BG256	256-Lead Ball Grid Array	
		CY37384VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37384VP256-66BGI	BG256	256-Lead Ball Grid Array	
512	83	CY37512VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-83BGC	BG256	256-Lead Ball Grid Array	
		CY37512VP352-83BGC	BG352	352-Lead Ball Grid Array	
		CY37512VP400-83BBC	BB400	400-Lead Fine-Pitch Ball Grid Array	
	66	CY37512VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-66BGC	BG256	256-Lead Ball Grid Array	
		CY37512VP352-66BGC	BG352	352-Lead Ball Grid Array	
		CY37512VP400-66BBC	BB400	400-Lead Fine-Pitch Ball Grid Array	
		CY37512VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512VP256-66BGI	BG256	256-Lead Ball Grid Array	
		CY37512VP352-66BGI	BG352	352-Lead Ball Grid Array	
		CY37512VP400-66BBI	BB400	400-Lead Fine-Pitch Ball Grid Array	
		5962-9952601QZC	U208	208-Lead Ceramic Quad Flat Pack	Military

Package Diagrams

44-Lead Thin Plastic Quad Flat Pack A44

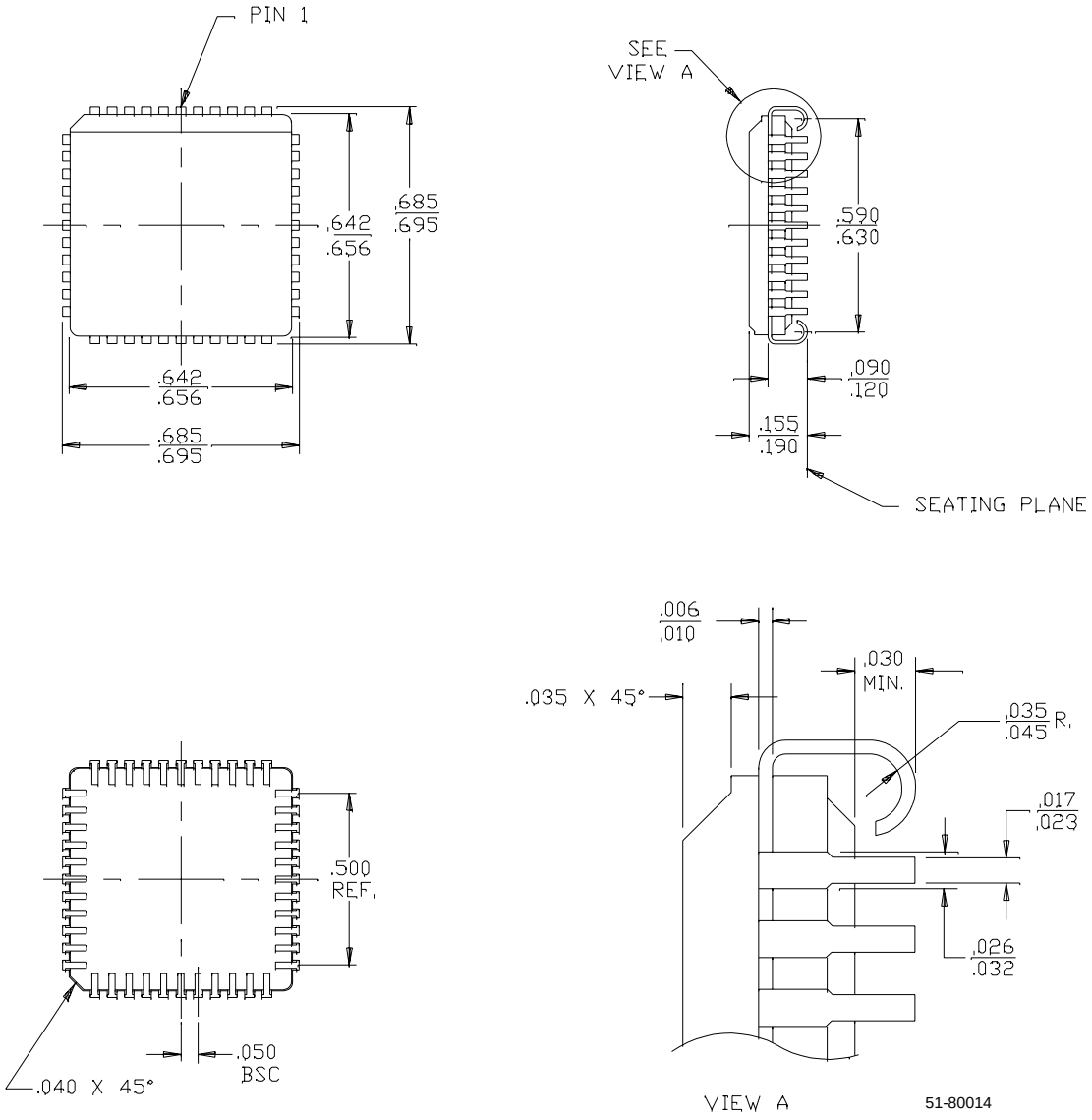


44-Lead Plastic Leaded Chip Carrier J67



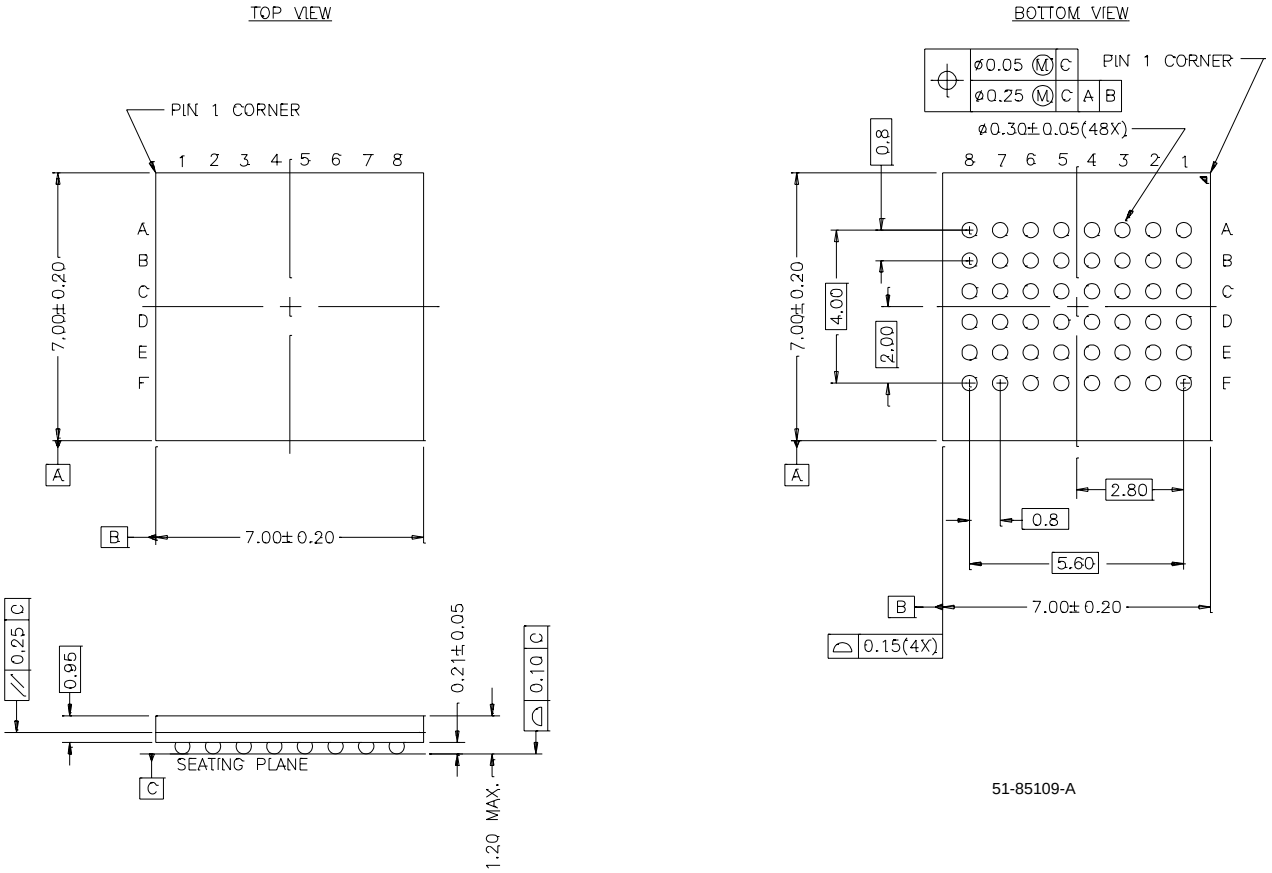
Package Diagrams (continued)

44-Pin Ceramic Leaded Chip Carrier Y67



Package Diagrams (continued)

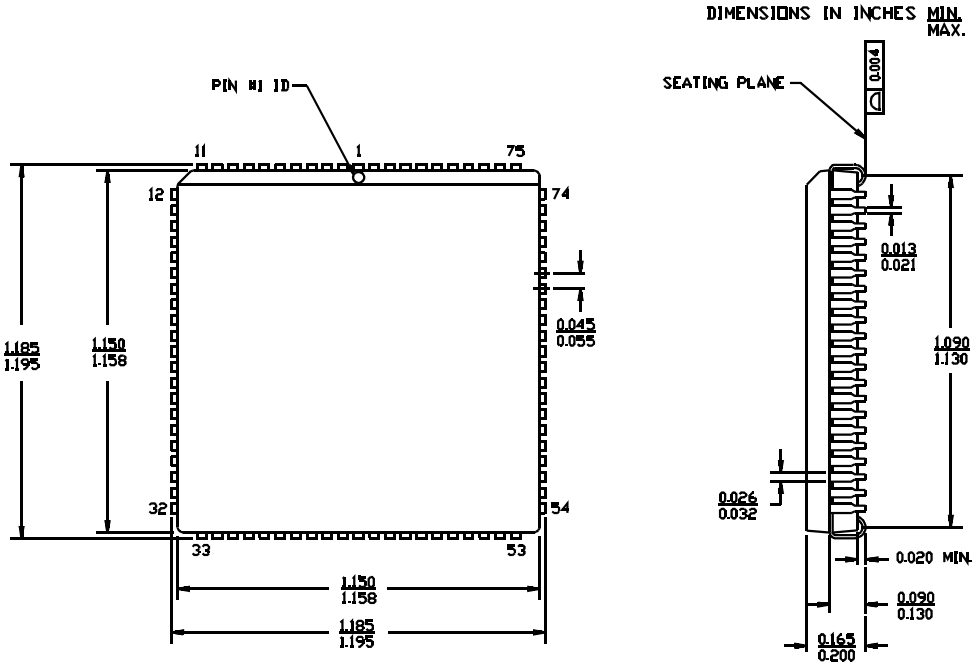
48-Ball (7.0 mm x 7.0 mm x 1.1 mm, 0.80 pitch) Thin BGA BA50



51-85109-A

Package Diagrams (continued)

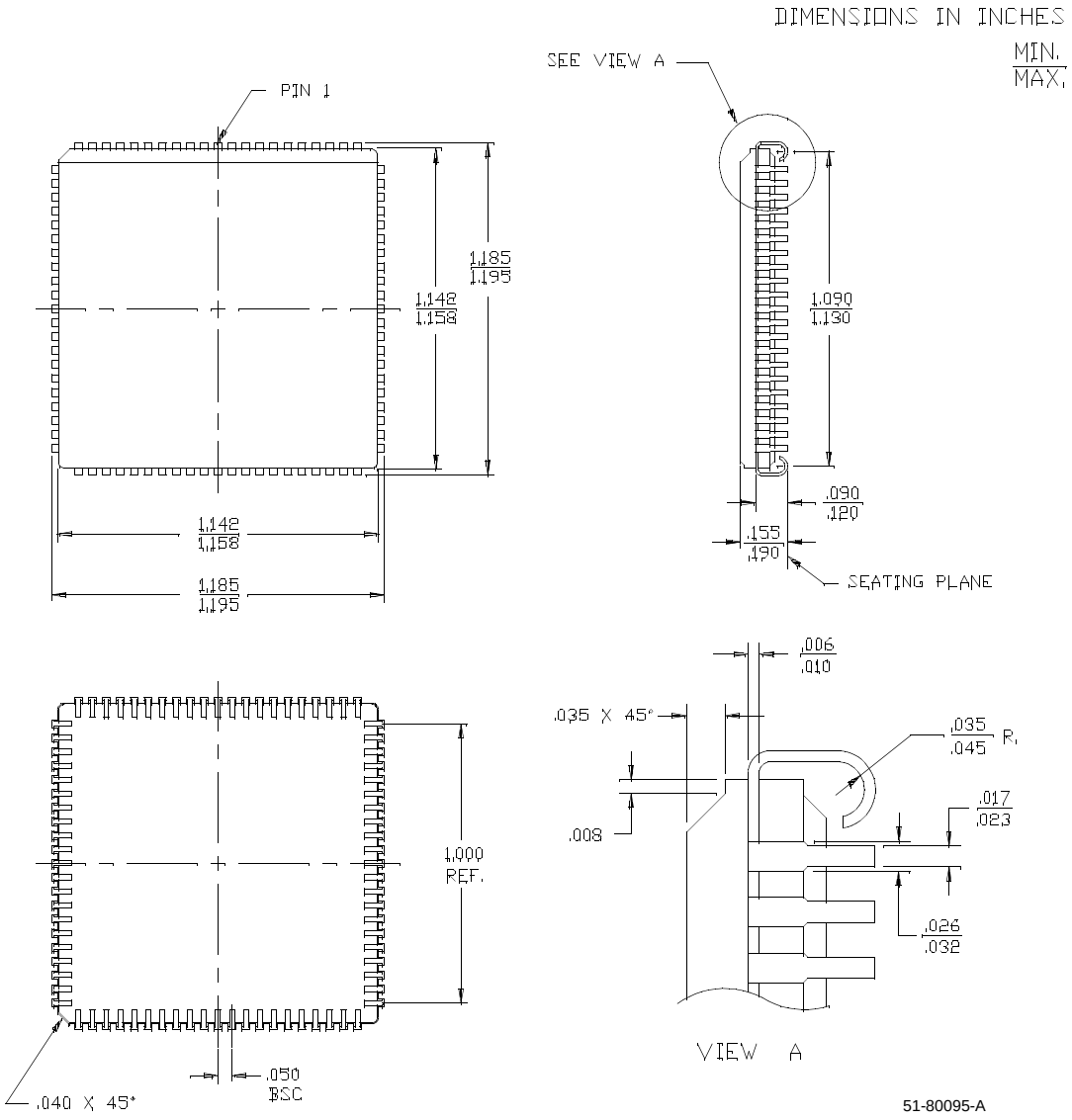
84-Lead Plastic Leaded Chip Carrier J83



51-85006-A

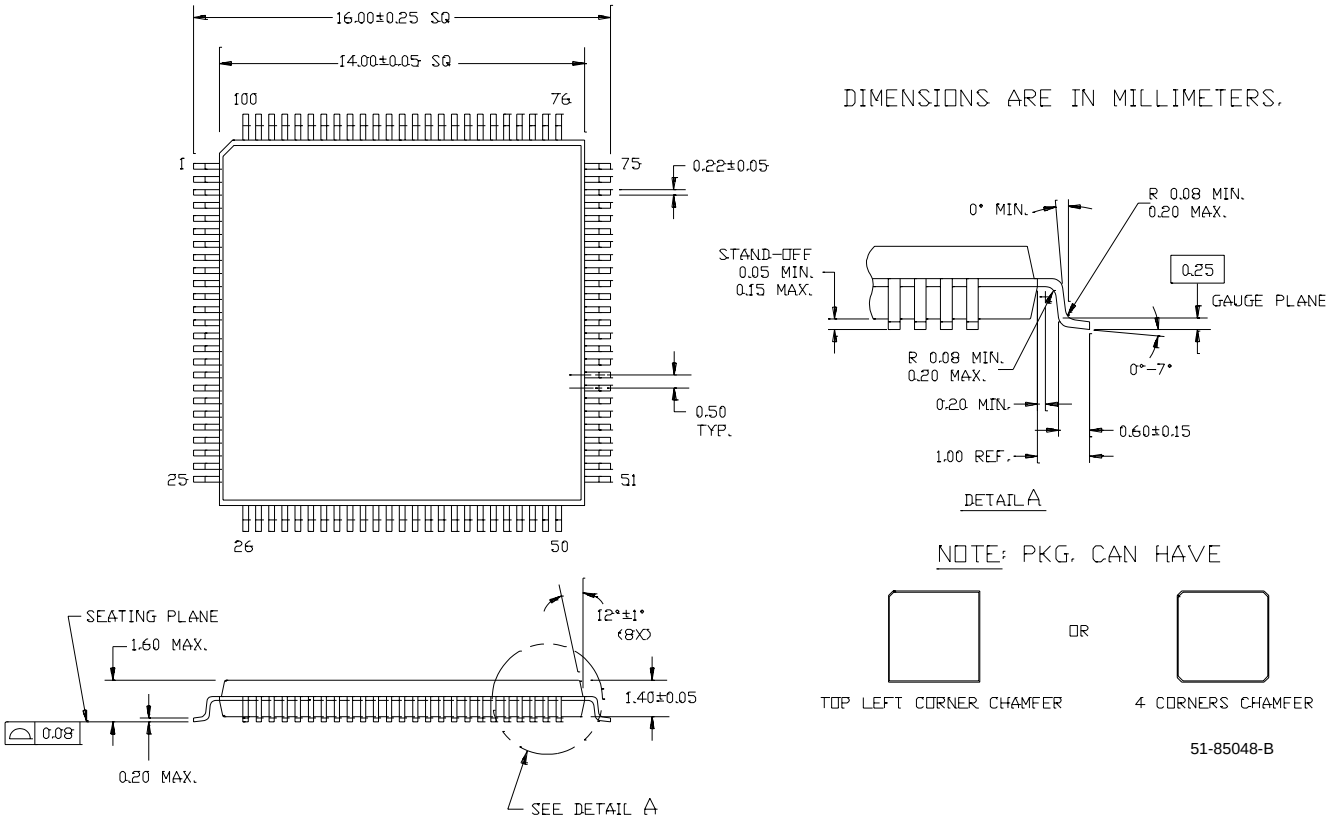
Package Diagrams (continued)

84-Pin Ceramic Leaded Chip Carrier Y84



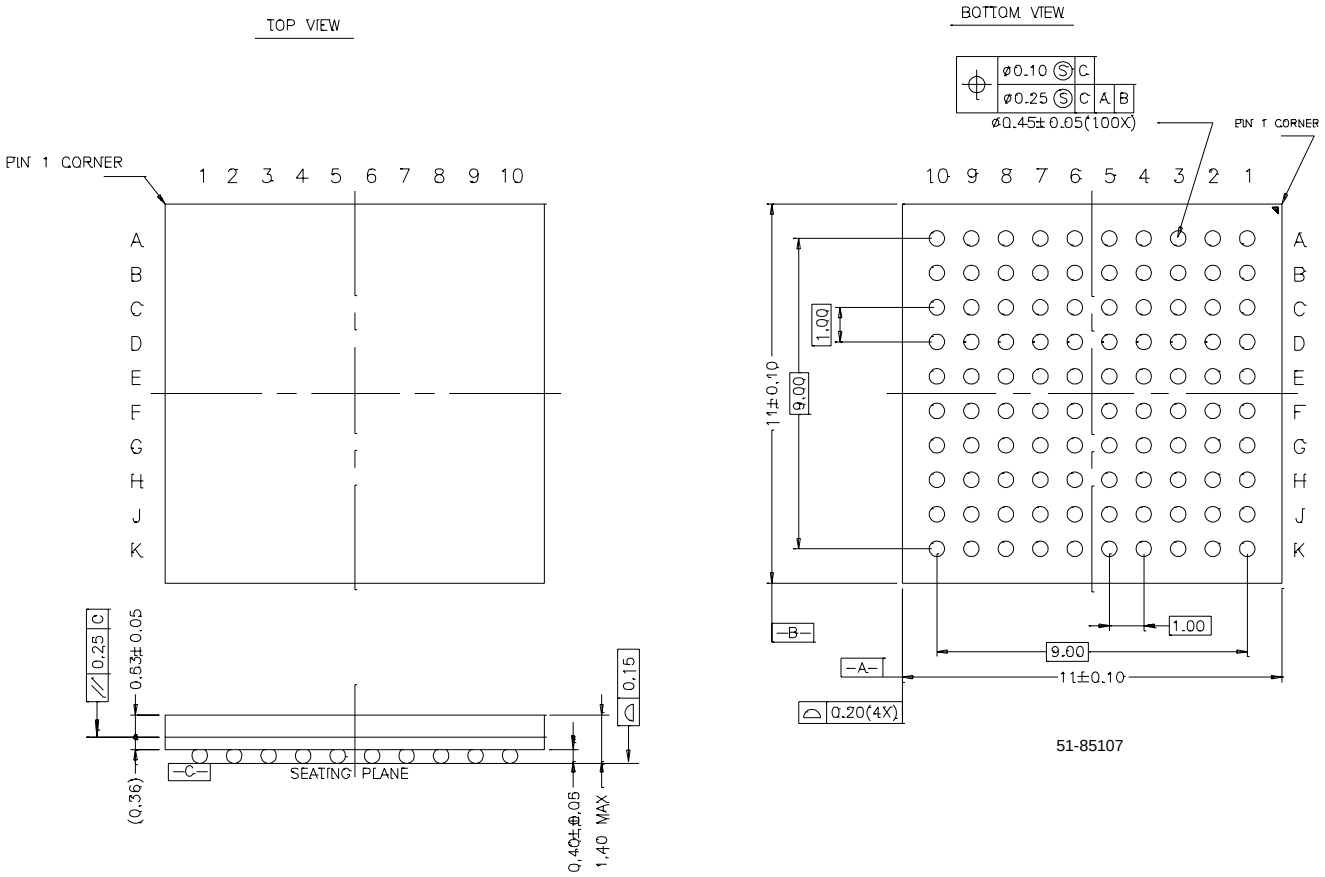
Package Diagrams (continued)

100-Pin Thin Plastic Quad Flat Pack (TQFP) A100



Package Diagrams (continued)

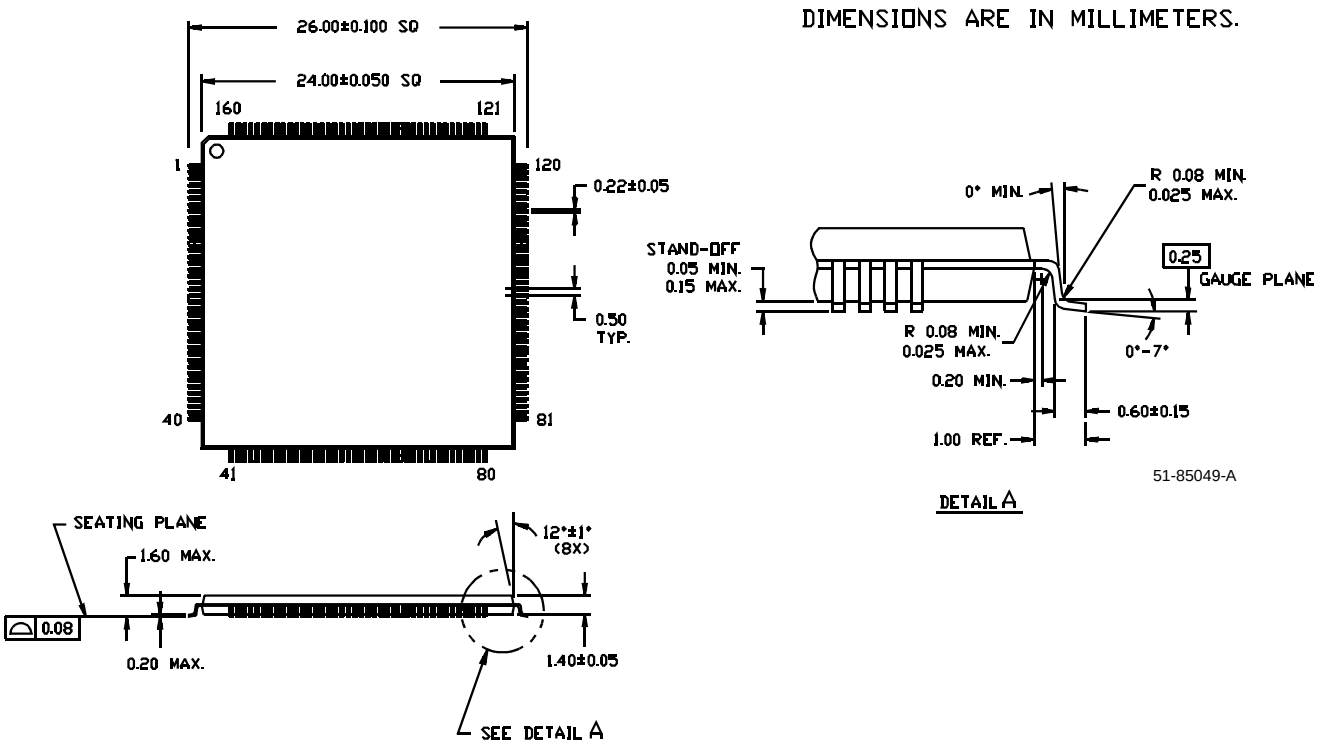
100-Ball Thin Ball Grid Array (11 x 11 x 1.4 mm) BB100



* THE BALL DIAMETER, BALL PITCH, STAND-OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC M0192 (LOW PROFILE BGA FAMILY)

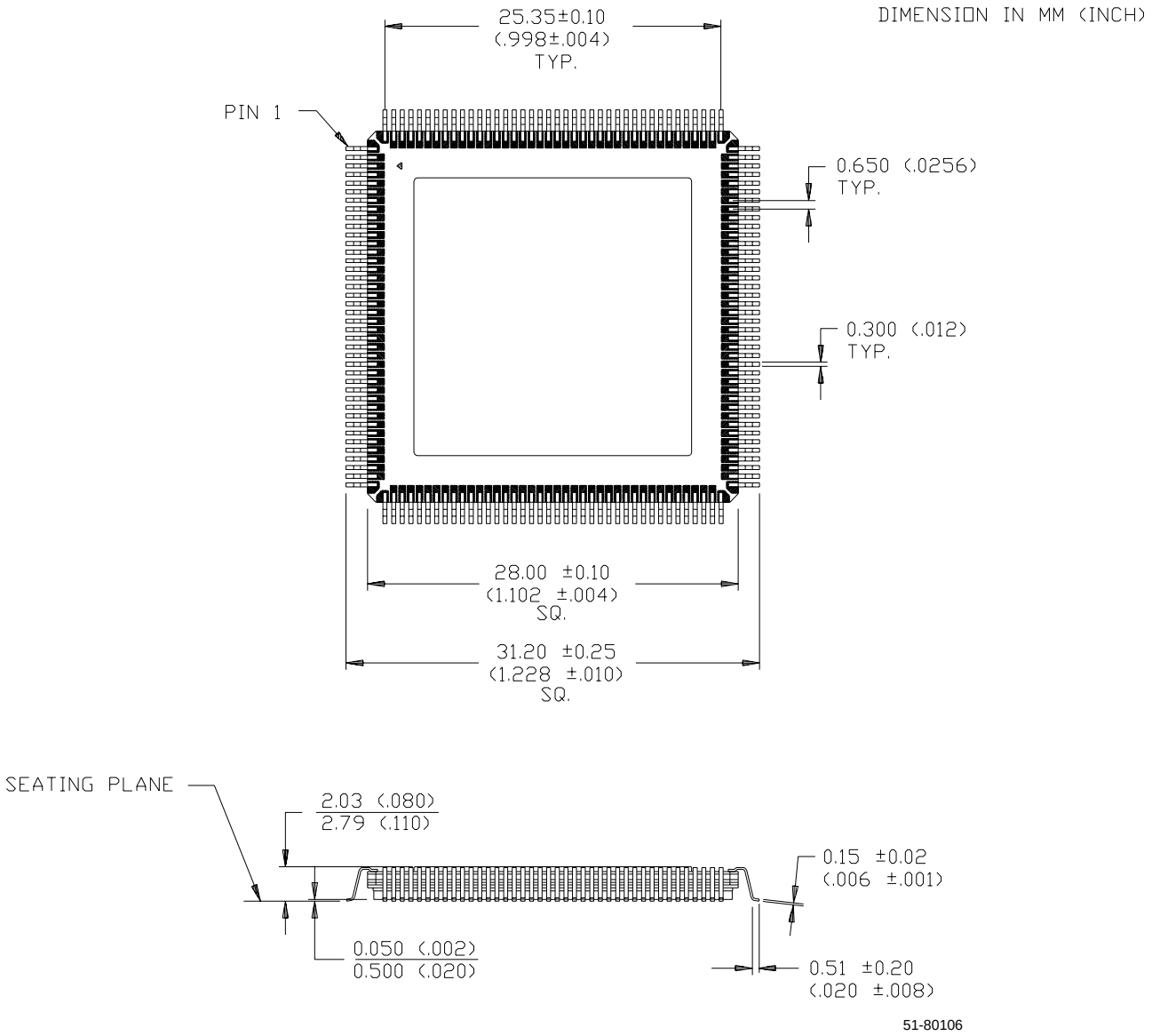
Package Diagrams (continued)

160-Pin Thin Plastic Quad Flat Pack (TQFP) A160



Package Diagrams (continued)

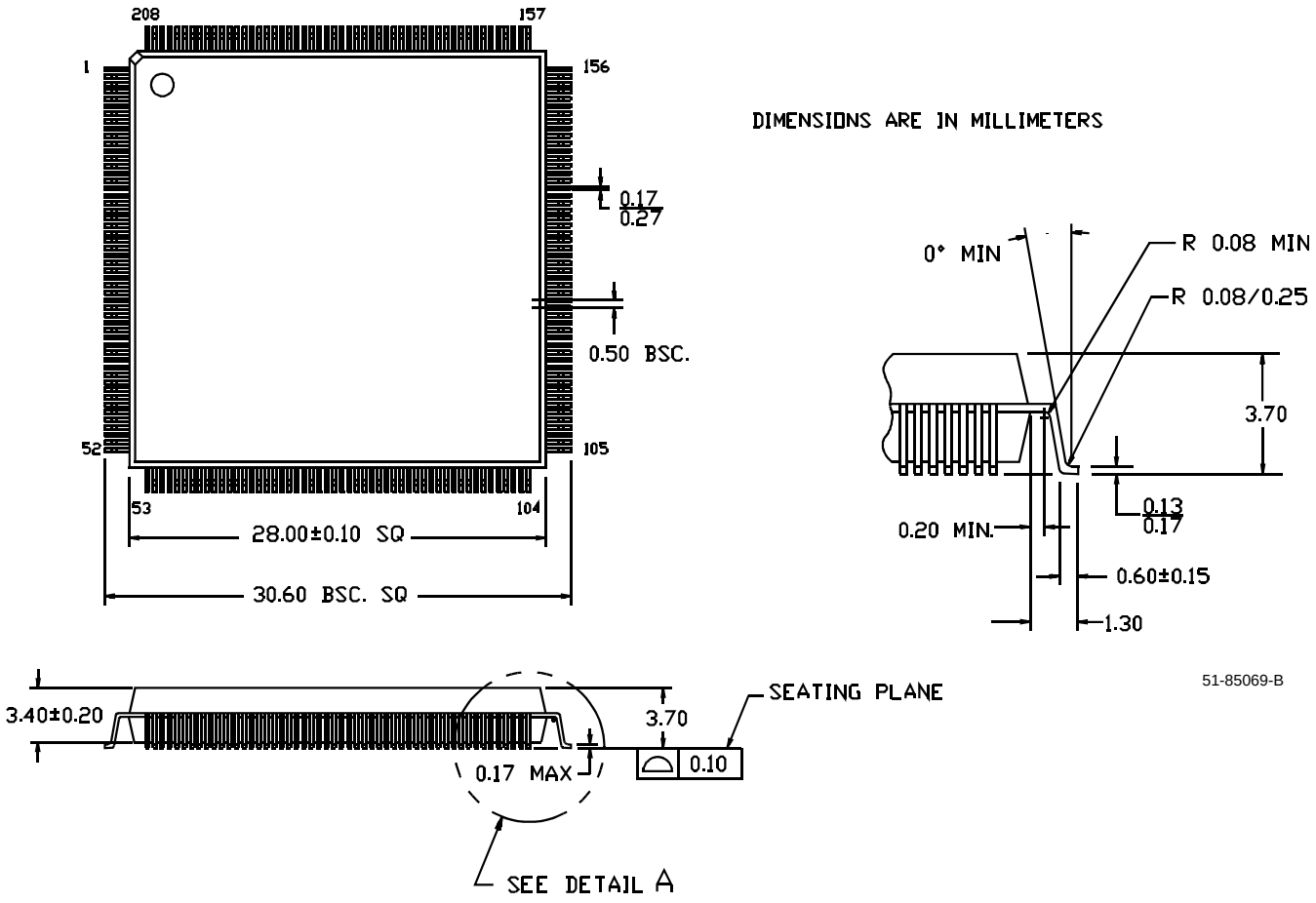
160-Lead Ceramic Quad Flatpack (Cavity Up) U162



51-80106

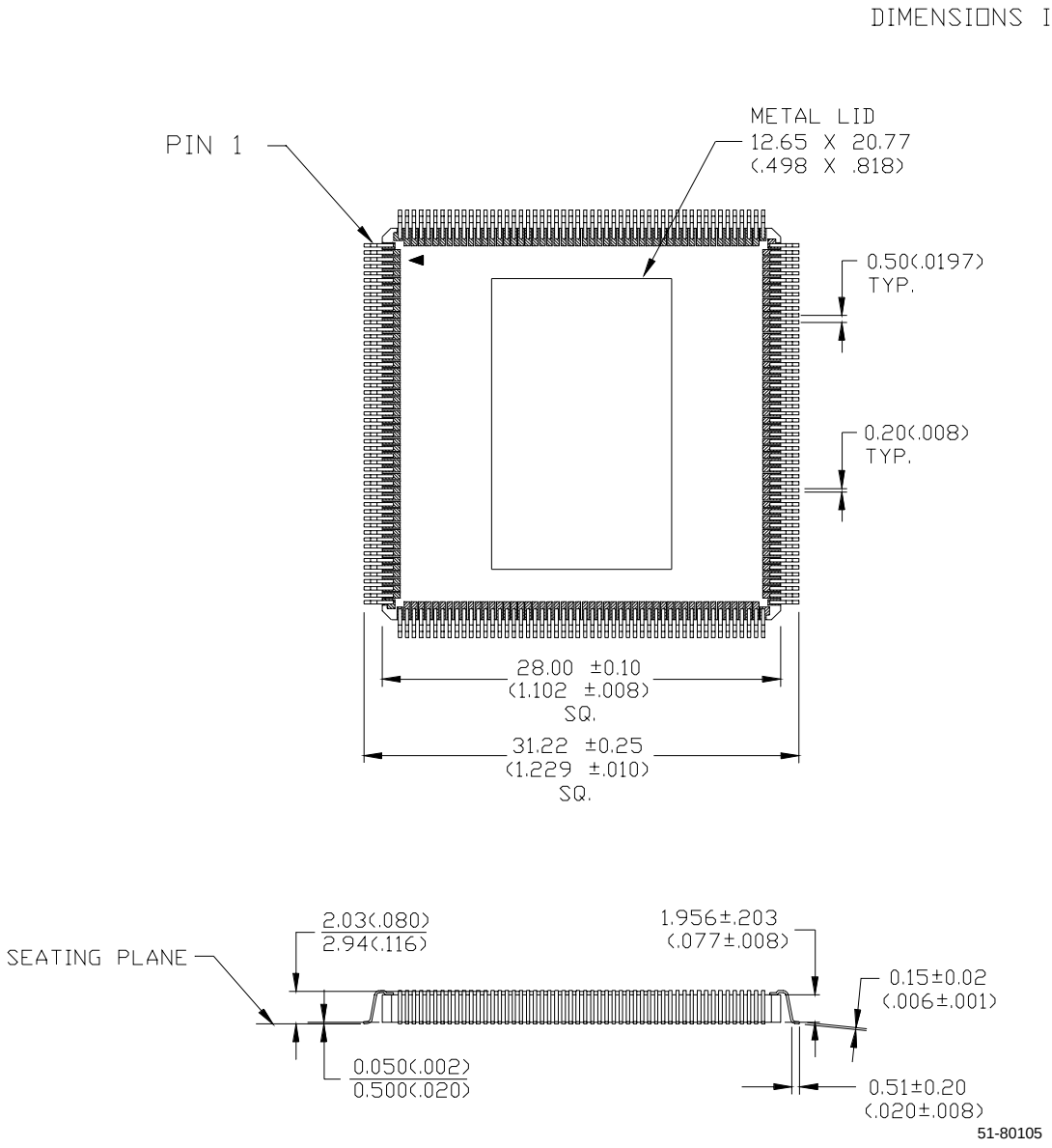
Package Diagrams (continued)

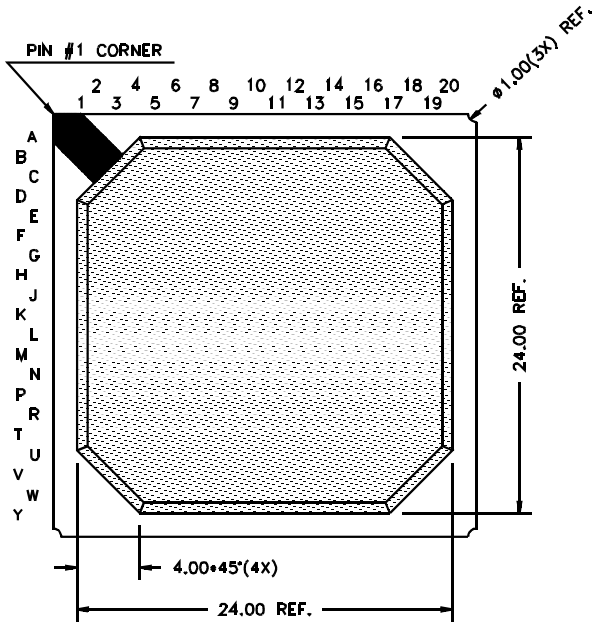
208-Lead Plastic Quad Flatpack N208

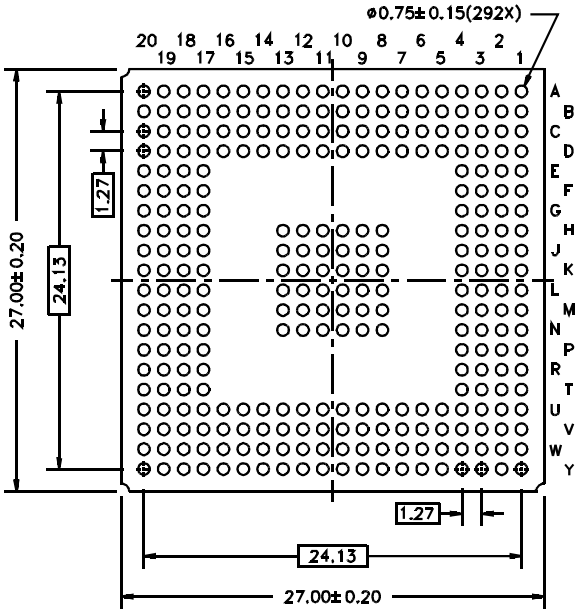


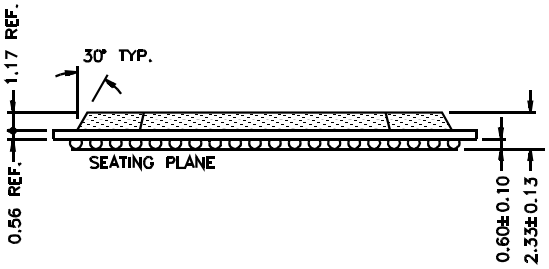
Package Diagrams (continued)

208-Lead Ceramic Quad Flatpack (Cavity Up) U208

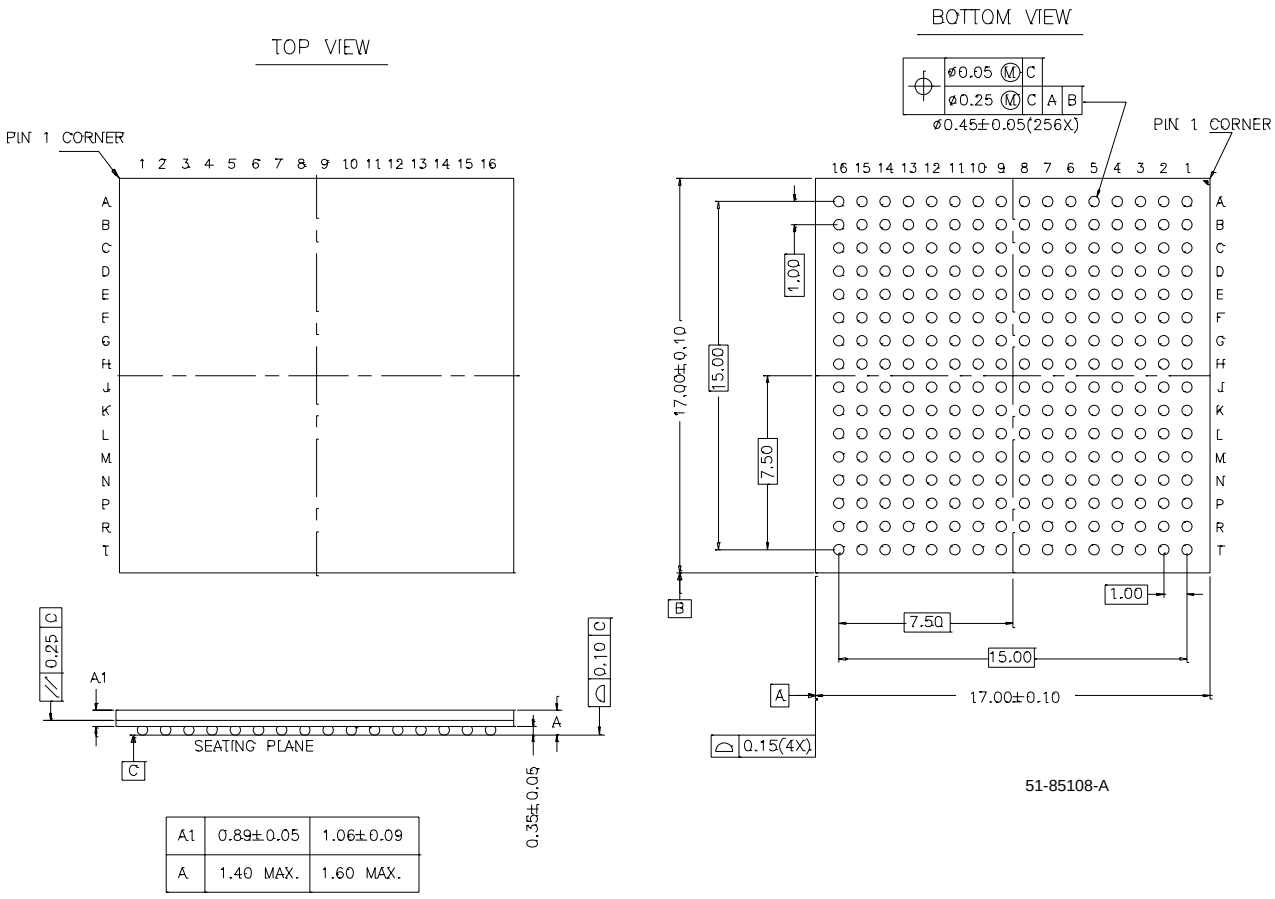



PIN #1 CORNER
ø1.00(3X) REF.
24.00 REF.
4.00•45°(4X)
24.00 REF.


ø0.75±0.15(292X)
1.27
24.13
27.00±0.20
1.27
24.13
27.00±0.20

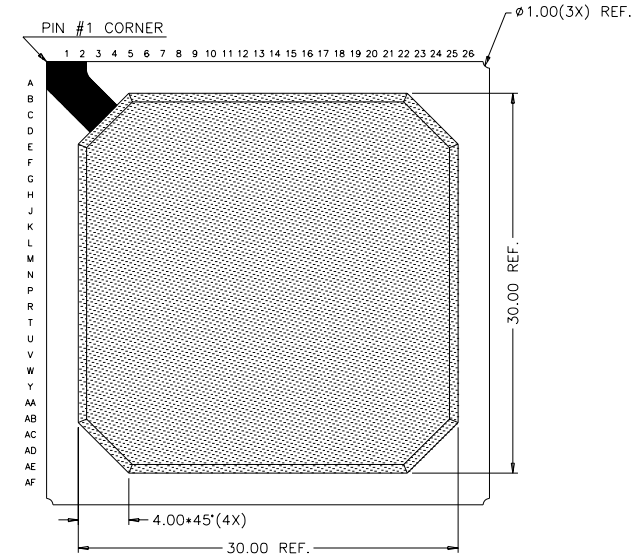

1.17 REF.
30° TYP.
SEATING PLANE
0.56 REF.
0.60±0.10
2.33±0.13

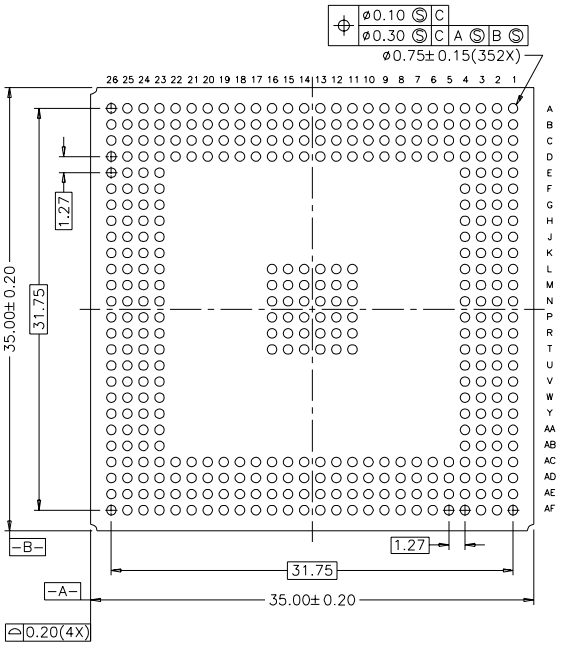
51-85097

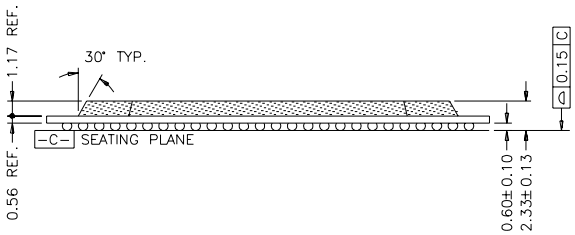


A1	0.89±0.05	1.06±0.09
A	1.40 MAX.	1.60 MAX.

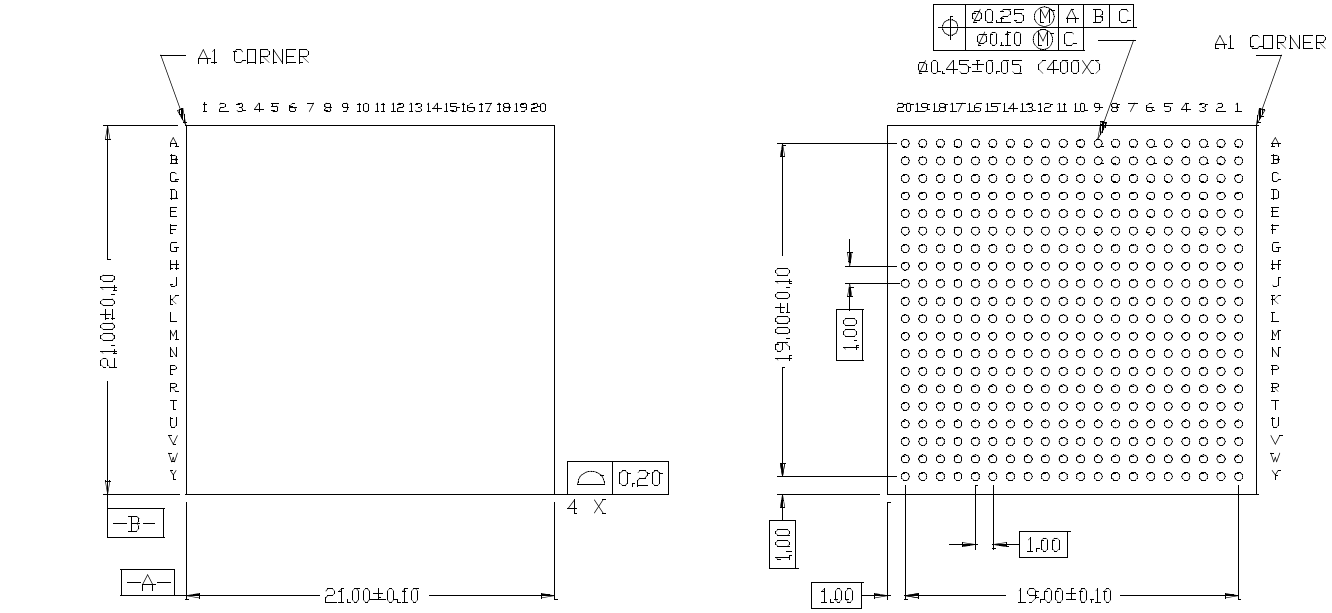
51-85108-A


PIN #1 CORNER
ø1.00(3X) REF.
30.00 REF.
4.00*45°(4X)
30.00 REF.


ø0.10 Ⓢ C
ø0.30 Ⓢ C A Ⓢ B Ⓢ
ø0.75± 0.15(352X)
1.27
31.75
35.00± 0.20
-B-
-A-
1.27
31.75
35.00± 0.20
0.20(4X)

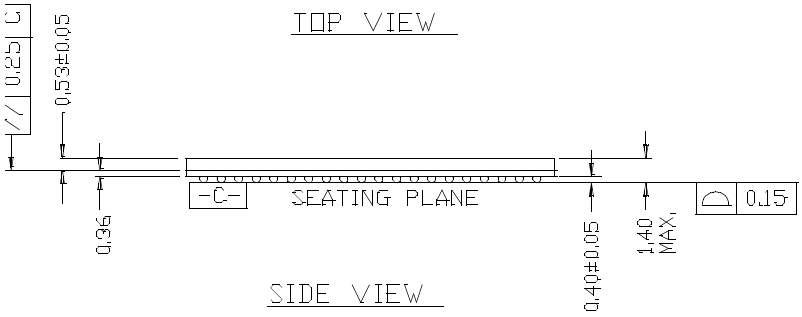

1.17 REF.
30° TYP.
0.15 C
-C- SEATING PLANE
0.56 REF.
0.60± 0.10
2.33± 0.13

51-85103



TOP VIEW

BOTTOM VIEW



SIDE VIEW

51-85111-A

**	106272	04/18/01	SZV	Change from Spec number: 38-00475 to 38-03007

5.5 PACDN005

Datasheet is encrypted and can not be added to file. See file pacdn005s.pdf.

5.6 PI49FCT

PI49FCT807T
PI49FCT2807T

Fast CMOS Clock Driver

Product Features

- Guaranteed low skew: 0.25ns
- Low input capacitance
- Minimum duty cycle distortion
- 1:10 fanout
- High speed: 3.5ns propagation delay
- TTL input and CMOS output compatible
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- Packages available:
  - 20-pin 300 mil wide SOIC (S)
  - 20-pin 150 mil wide QSOP (Q)
  - 20-pin 209 mil wde SSOP (H)
- Industrial Operation at -40ºC to +85ºC

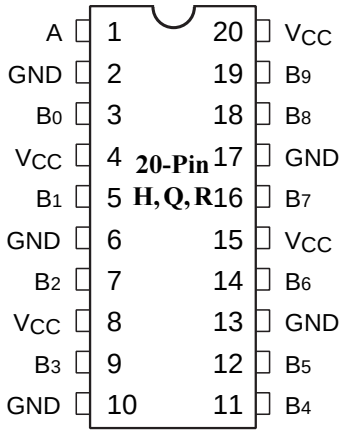
Product Description

Pericom Semiconductor's PI49FCT series of logic circuits are produced using the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

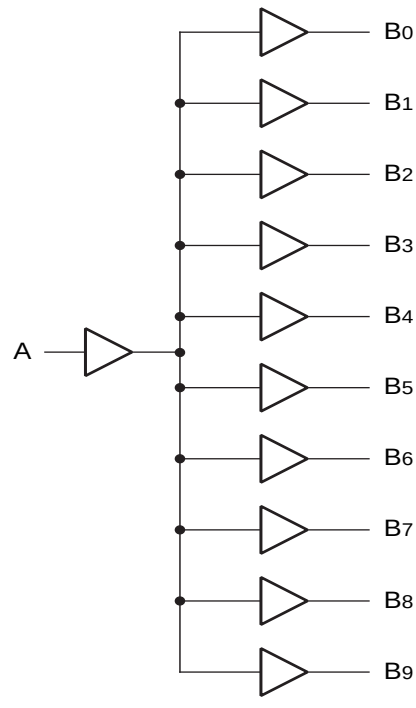
The PI49FCT807T and PI49FCT2807T clock drivers feature one input and ten outputs. The large fanout from a single input line reduces loading on input clock. TTL level outputs reduce noise levels on the part. Typical applications are clock and signal distribution.

The PI49FCT2807T also features a 25-ohm on-chip resistor for lower noise.

Product Pin Configuration



Logic Block Diagram



Product Pin Description

Pin Name	Description
A	Input
B0 – B9	Outputs
GND	Ground
V_{CC}	Power

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, $T_A = –40°C$ to $+85°C$, $V_{CC} = 5.0V \pm 5\%$)

Parameters	Description	Test Conditions[1]		Min.	Typ.[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = –15.0mA$	2.4	3.3		V
			$I_{OH} = 48.0mA$		0.2	0.5	V
V_{OL}	Output LOW Current	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 12mA (25\Omega)$		0.2	0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	$V_{IN} = 2.7V$			1	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	$V_{IN} = 0.5V$			–1	µA
I_I	Input HIGH Current	V_{CC} = Max., $V_{IN} = V_{CC}$ (Max.)				20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., $I_{IN} = –18mA$			–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND		–60	–120	–225	mA
I_{OFF}	Power Down Disable	V_{CC} = GND, $V_{OUT} = 4.5V$		—	—	100	µA
V_H	Input Hysteresis				150		mV

Capacitance ($T_A = 25°C$, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ.	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6.0	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ.[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or Vcc		3	30	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.,	V_{IN} = 3.4V[3]		0.5	1.5	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open 50% Duty Cycle, One Input Toggling	V_{IN} = V_{CC} V_{IN} = GND		0.4	0.6	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 50 MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		20	30[5]	mA
			V_{IN} = 3.4V V_{IN} = GND		20.7	33[5]	

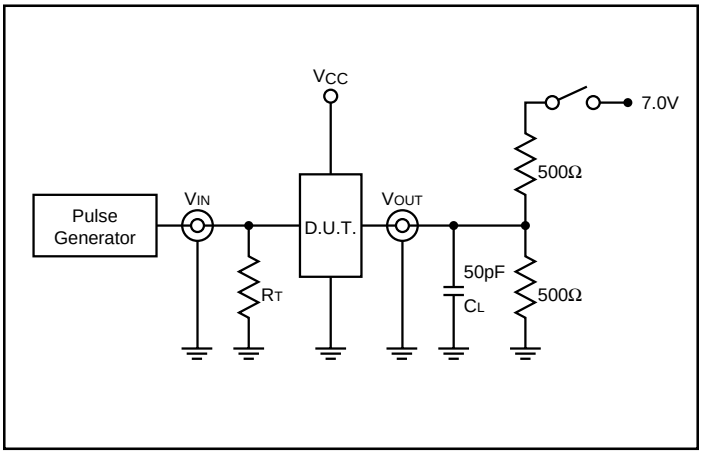
Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_I = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	807/2807T Com. Min.	807/2807T Com. Max.	807AT Com. Min.	807AT Com. Max.	807BT Com. Min.	807BT Com. Max.	807CT Com. Min.	807CT Com. Max.	Units
t_{PLH} t_{PHL}	Propagation Delay A to B_N	C_L = 50pF R_L = 500Ω	1.5	4.5	1.5	4.0	1.5	3.8	1.5	3.5	ns
$t_{SK(o)}$	Skew between two outputs of same package[3]		—	0.5	—	0.5	—	0.35	—	0.25	ns
$t_{SK(p)}$	Skew between opposite transitions of same output ($\lvert t_{PHL} - t_{PLH} \rvert$)[3]		—	0.5	—	0.5	—	0.35	—	0.35	ns
$t_{SK(t)}$	Skew between outputs of different package at same power supply, temperature and speed grade[3]		—	1.0	—	1.0	—	0.75	—	0.75	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

Tests Circuits For All Outputs(1)



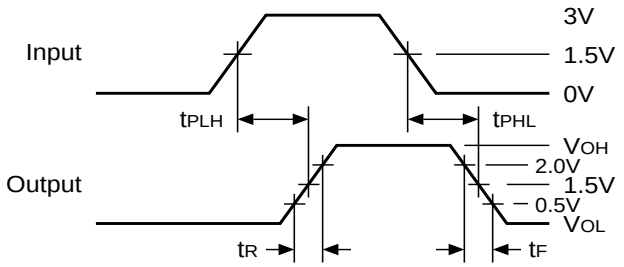
Switch Position

Test	Switch
Open Drain Disable LOW Enable LOW	Closed
All Other Inputs	Open

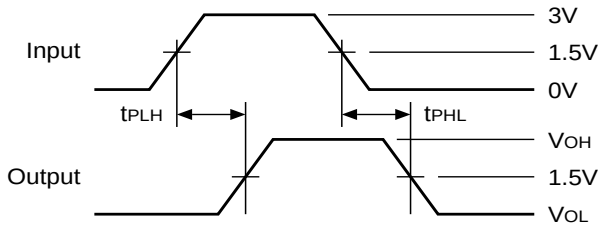
Definitions:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to ZOUT of the Pulse Generator.

Switching Waveforms

Propagation Delay

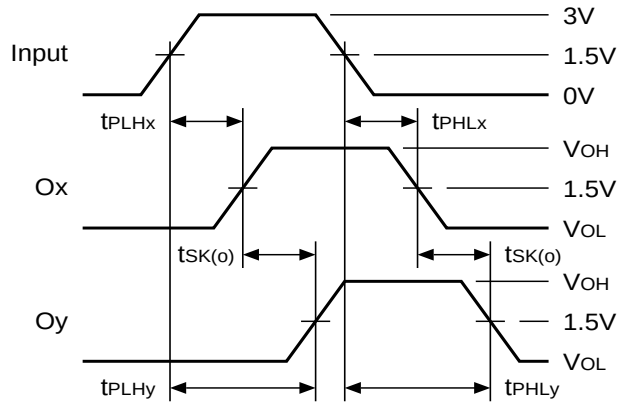


Pulse Skew – $t_{SK(p)}$



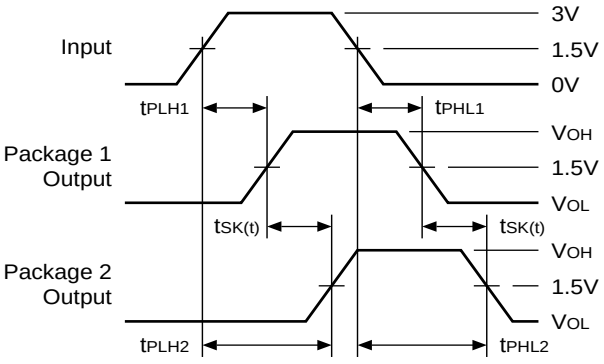
$t_{SK(p)} = |t_{PHL} - t_{PLH}|$

Output Skew – $t_{SK(o)}$



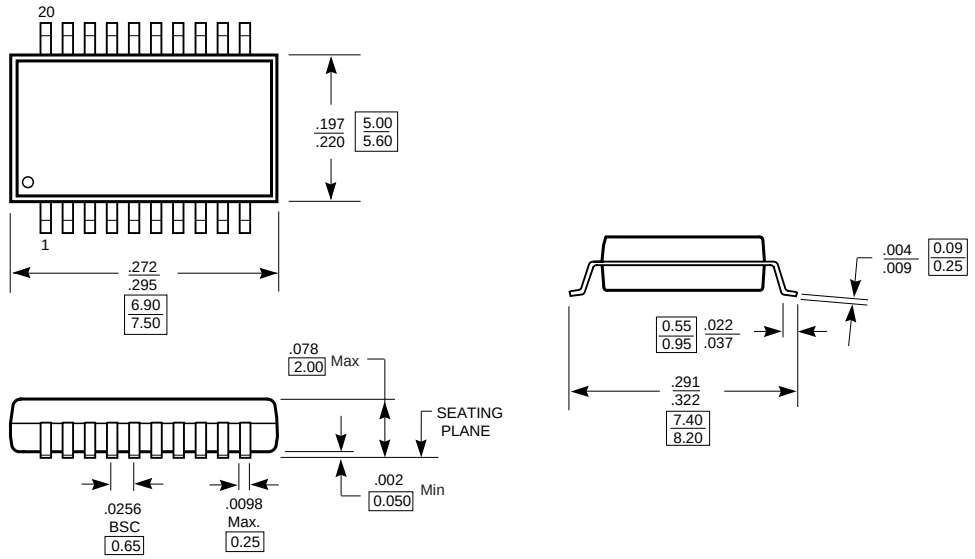
$t_{SK(o)} = |t_{PLHy} - t_{PLHx}|$ or $|t_{PHLy} - t_{PHLx}|$

Package Skew – $t_{SK(t)}$

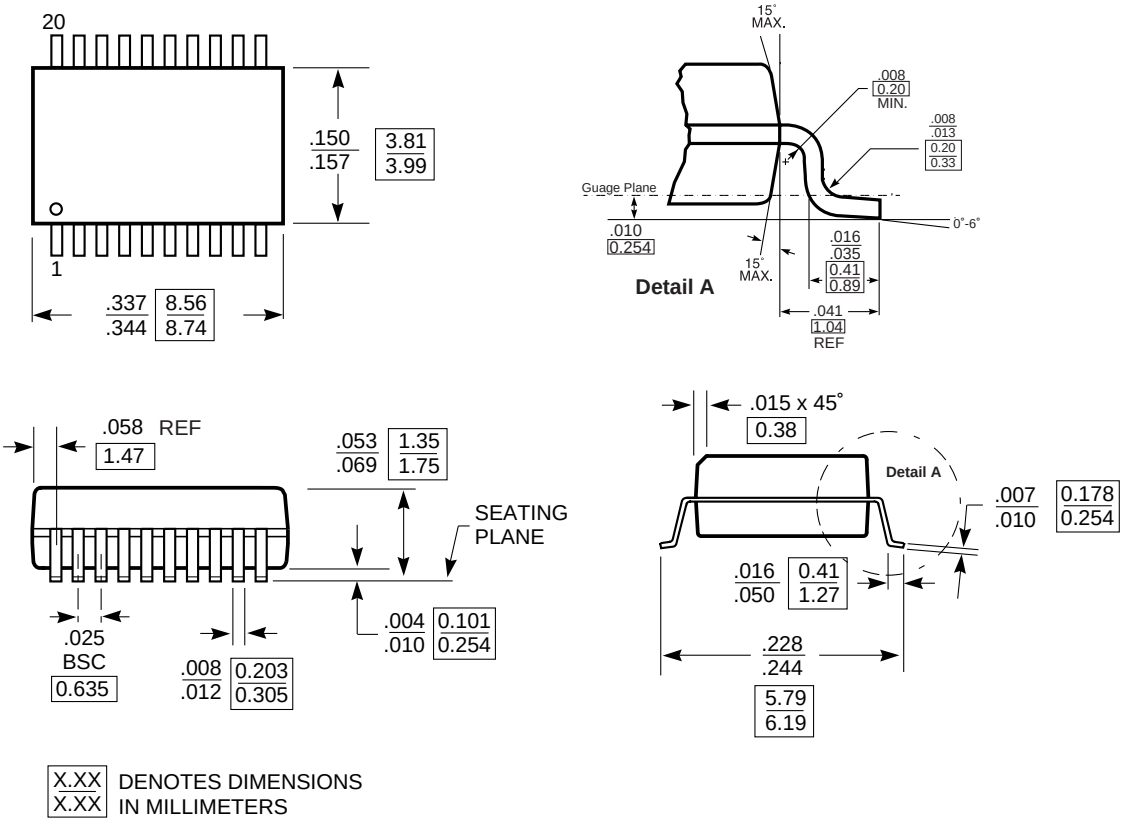


$t_{SK(t)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

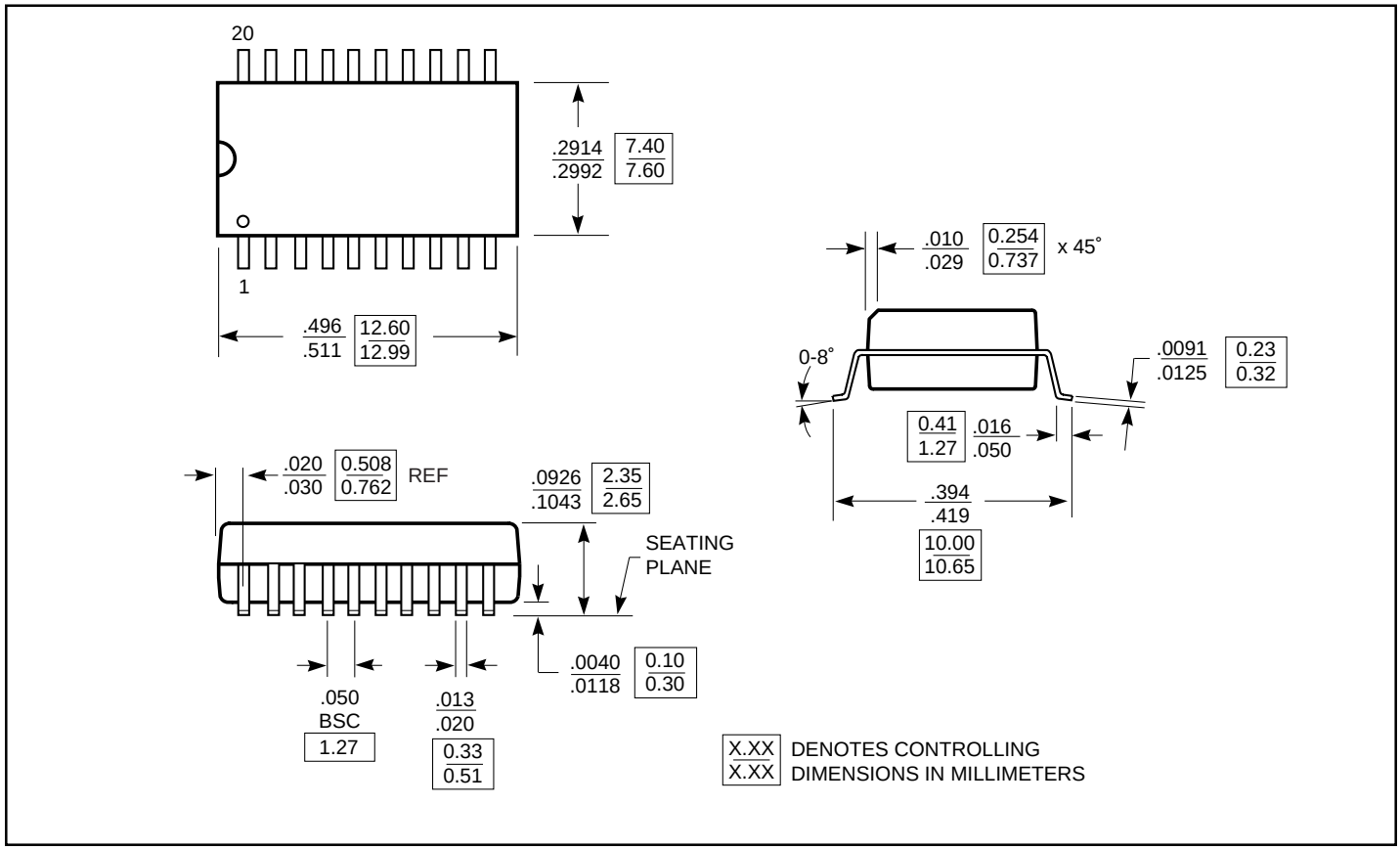
20-Pin 209-Mil SSOP (H)



20-Pin 150-Mil QSOP (Q)



20-Pin 300-Mil SOIC (S)



Ordering Information

Part Number	Marking Code
PI49FCT807xTp	PI49FCT807Tpx
PI49FCT2807Tp	PI49FCT2807Tp

Note: x = Speed Grades: "blank", A, B, C.
p = Package Type:
H = 209-mil SSOP
Q = 150-mil QSOP
S = 300-mil SOIC

Example:
PI49FCT807ATH = A grade,
H pkg marked as PI49FCT807THA